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Study on the charge trapping phenomena in silicon carbonitride films for nonvolatile semiconductor memory applications

（不揮発性半導体メモリへの応用のためのシリコン炭窒化膜の電荷捕獲現象
に関する研究）

指導教員　　小林清輝　教授

東海大学大学院　総合理工学研究科
総合理工学専攻

SHEIKH RASHEL AL AHMED

Dedicated To

My Parents and My Son

Abstract

The metal-oxide-nitride-oxide-semiconductor (MONOS)-type memory with an ultrathin tunnel oxide film has attracted significant attention for embedded nonvolatile memory (NVM) applications. Electrons and holes captured by charge trap centers existing in the silicon nitride charge trapping film induce a shift in the threshold voltage of memory transistors in the MONOS-type devices. This phenomenon is applied to store data. The memory cell size in the MONOS-type devices has been becoming smaller in the past few decades. In such small memory cells, it is a challenge to promote the programming and erasing speeds and data retention simultaneously. Therefore, a better understanding of the electron and hole trapping mechanisms and of the emission mechanism of carriers trapped in the charge trapping films is important.

In this dissertation, the constant-current carrier injection method was proposed to analyze the charge centroid of carriers trapped in the charge trapping films and to count the number of carriers injected to the films. Recently, silicon carbonitride (SiCN) dielectric film has been expected to be an attractive candidate of the charge trapping film of embedded NVMs instead of the silicon nitride film. Unfortunately, there are few reports on the charge trapping phenomenon in the SiCN-based memory. Therefore, a comparative study of the charge centroid of holes captured by empty trap centers in the SiCN and silicon nitride charge trapping films was made using the proposed constant-current hole injection method and the hole transport in both films was discussed also. The charge centroid of trapped holes was initially located near the middle of the SiCN and silicon nitride films, and then moved to the vicinity of the blocking oxide films with increasing the number of holes injected to the charge trapping films. It was also found that the charge centroid of holes trapped in the SiCN film was closer to the blocking oxide film as compared to that in the silicon nitride film. These experimental results were explained by taking into account the Poole-Frenkel conduction of holes in the charge trapping films.

The electron elimination phenomena in the SiCN and silicon nitride charge trapping films with trap centers filled by electrons was also investigated by using the constant-current carrier injection method. It was found that almost all electrons trapped in the charge trapping films could be eliminated due to hole injection under negative gate bias.

In addition, in the present study, an improved analytical method for the charge retention characteristics in the charge trapping films was presented. This method allows us to extract the energy distribution of charge carriers trapped in the SiCN or new dielectric films without using any adjustable parameters. Using the proposed method, the trapped electrons were determined to be distributed from 0.8 to 1.3 eV below the conduction band edge in the SiCN charge trapping film. In the view point of the charge retention, the presence of such deep trap centers lead us to suggest that the SiCN dielectric films can be employed as the charge trapping film of embedded NVMs.

In this study, the constant-current carrier injection method and the analytical method for the charge retention characteristics in the charge trapping films were proposed. It is shown that the constant-current carrier injection method is useful for obtaining the accurate charge centroid of carriers trapped in the charge trapping films. The experimental results and discussion shown in this dissertation are important to get a better understanding of the hole trapping phenomena in the SiCN and silicon nitride charge trapping films. From the view point of the charge retention of NVMs, the proposed analytical method for the charge retention characteristics, which needs no adjustable and extra parameters, is helpful for determining the energy distribution of carriers trapped in the SiCN or new dielectric films. The two methods proposed in the present study are considered to be advantageous to develop embedded NVMs employing the SiCN or new charge trapping films.

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List of Abbreviations

Abbreviation	Description
AFM	Atomic force microscopy
CB	Conduction band
CMOS	Complementary metal-oxide-semiconductor
CV	Capacitance-voltage
ESR	Electron spin resonance
FN	Fowler-Nordheim
HI-BK	Hole injection following the baking
HI-EI	Hole injection following the electron injection
I_d-V_g	Drain current-gate voltage
J_g-V_g	Gate current density-gate voltage
LPCVD	Low-pressure chemical vapor deposition
MCUs	Microcontroller units
MONOS	Metal-oxide-nitride-oxide-semiconductor
NVMs	Nonvolatile memories
PECVD	Plasma-enhanced chemical vapor deposition
PF	Poole-Frenkel
SiCN	Silicon carbonitride
XPS	X-ray photoelectron spectroscopy

List of Symbols

Symbol	Unit used in this dissertation	SI unit	Description
C_{ox}	[F/m^2]		Capacitance per unit area of a gate electrode-blocking oxide-silicon nitride-tunnel oxide-silicon structure
$D(t,T,\Phi_E)$	[m^{-3}eV^{-1}]	[m^{-3}J^{-1}]	Number of filled trap centers per unit volume and unit energy
E	[V/m]		Electric field
$\overline{E}$	[V/m]		Average electric field
E_{box}	[V/m]		Electric field in the blocking oxide film
ΔE_{fix}	[V/m]		Electric field in the blocking oxide film induced by the fixed positive charge
ΔE_{hole}	[V/m]		Electric field in the blocking oxide film induced by trapped holes
ε_{box}			Static relative dielectric constant of the blocking oxide film
ε_{ctl}			Static relative dielectric constant of the charge trapping film
ε_d			Dynamic relative dielectric constant
ε_0	[F/m]		Permittivity of free space
F_{inj}	[m^{-2}]		Number of injected holes per unit area
$f(t,T)$			Occupancy function
Φ_b	[J]		Energy barrier height for electrons
Φ_E	[eV]	[J]	Energy depth of trap centers
Φ_{EH}	[eV]	[J]	Highest energy level of trap centers
Φ_{EL}	[eV]	[J]	Lowest energy level of trap centers
ϕ_{ms}	[V]		Metal-semiconductor work function deference
ϕ_F	[V]		Fermi potential
ϕ_t	[V]		Energy depth of trap centers

h	[Js]		Planck constant
$\hbar$	[Js]		Reduced Planck constant
I_d	[A]		Drain current
J_{FN}	[A/m^2]		Fowler-Nordheim (FN) tunneling current
J_g	[A/m^2]		Gate current density
$J_{leak}(t)$	[A/m^2]		Leakage current component owing to electron and hole flows across the stacked dielectric films
$J_{sub}(t)$	[A/m^2]		Displacement current component owing to hole accumulation at silicon surface
$J_{trap}(t)$	[A/m^2]		Displacement current component owing to hole trapping by trap centers existing in the charge trapping film
k_B	[eV/K]	[J/K]	Boltzmann constant
$N(t,T)$	[m^{-3}]		Number of filled trap centers per unit volume at retention time t for testing temperature T
m	[kg]		Electron mass in free space
m_{ox}	[kg]		Electron mass in SiO$_2$
P			Probability of the Poole-Frenke (PF) emission of holes from trap centers
Q_B	[C/m^2]		Charge per unit area in the depletion region of the silicon surface
$Q_{inj}(t_0,t_1)$	[C/m^2]		Injected charge per unit area
$Q_{sub}(t_0,t_1)$	[C/m^2]		Accumulation of holes at the silicon surface after hole injection
$Q_{trap}(t_0,t_1)$	[C/m^2]		Density of trapped charge
q	[C]		Elementary charge
R_a	[nm]	[m]	Arithmetic mean roughness
R_q	[nm]	[m]	Root-mean-square roughness
T	[K]		Temperature
t	[s]		Carrier injection time or Retention time
t_{box}	[m]		Thickness of the blocking oxide film
t_{ctl}	[m]		Thickness of the charge trapping film
t_{eq}	[m]		Oxide-equivalent thickness of stacked

		films
t_{tn}	[m]	Thickness of the tunnel oxide film
$\tau(T,\Phi_E)$	[s]	Time constant of thermal excitation of electrons
τ_0	[s]	Pre-exponential coefficient of the time constant for thermal excitation
V_{fb}	[V]	Flat-band voltage
$V_{fb,0}$	[V]	Flat-band voltage after baking at 235 °C
$V_{fb,e1}$	[V]	Flat-band voltage after electron trapping
$V_{fb,h1}$	[V]	Flat-band voltage after hole trapping
$V_{fb}(t,T)$	[V]	Flat-band voltage at retention time t for the testing temperature T
V_g	[V]	Gate voltage
V_{th}	[V]	Threshold voltage
$\Delta V_{fb,h}$	[V]	Flat-band voltage shift due to trapped holes
$\bar{x}_{fix}$	[m]	Charge centroid of fixed positive charge
$\bar{x}_{tctl}$	[m]	Charge centroid of carriers trapped in the charge trapping film

Chapter 1

Introduction

Chapter 1 Introduction

1.1 Embedded nonvolatile semiconductor memories

Microcontroller units (MCUs) with embedded nonvolatile memories (NVMs) have been widely used in automotive and consumer applications. The embedded NVM is defined as the NVM that is physically and electrically integrated into the MCUs. The embedded NVMs offer the following advantages to the MCUs: higher system speed, low system cost, low power consumption, and improved security.

The metal-oxide-nitride-oxide-semiconductor (MONOS)-type device with an ultrathin tunnel oxide film has received considerable interest for embedded NVM applications [1-10]. Figure 1.1 shows the schematic cross-section of the typical MONOS-type memory device. Blocking oxide-silicon nitride-tunnel oxide stacked dielectric films are located between the gate electrode and silicon substrate. There are several advantages in the MONOS-type devices such as low programming and erasing voltages, excellent
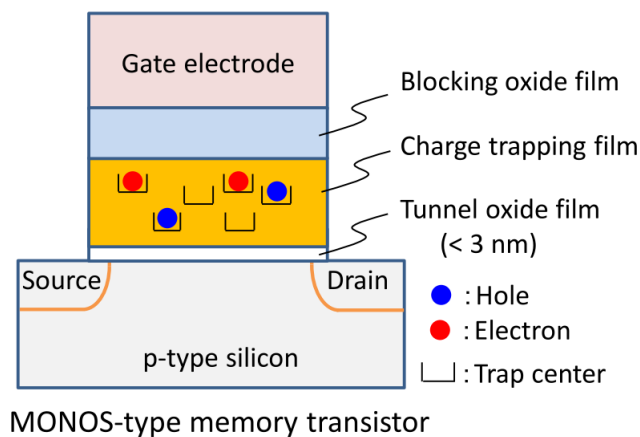
Fig. 1.1 Schematic cross-section of the MONOS-type memory transistor.

compatibility with the standard complementary metal-oxide-semiconductor (CMOS) process, good scalability and low cost [9,10].

The MONOS-type devices can store information by capturing charges in trap centers distributed in the silicon nitride charge trapping film. During programming and erasing operations, the threshold voltage V_{th} of the MONOS-type memory transistors is shifted by electrons and holes trapped in the silicon nitride film, as shown in Fig. 1.2. The equation for V_{th} is given by [11]

$$V_{th} = V_{fb} + 2\phi_F + \frac{Q_B}{C_{ox}} ,$$
(1.1)

where V_{fb} is the flat-band voltage, ϕ_F is the fermi potential, Q_B is the charge per unit area in the depletion region of the silicon surface, and C_{ox} is the capacitance per unit area of the gate electrode-blocking oxide-silicon nitride-tunnel oxide-silicon structure.

There are several charge injection mechanisms in programming and erasing
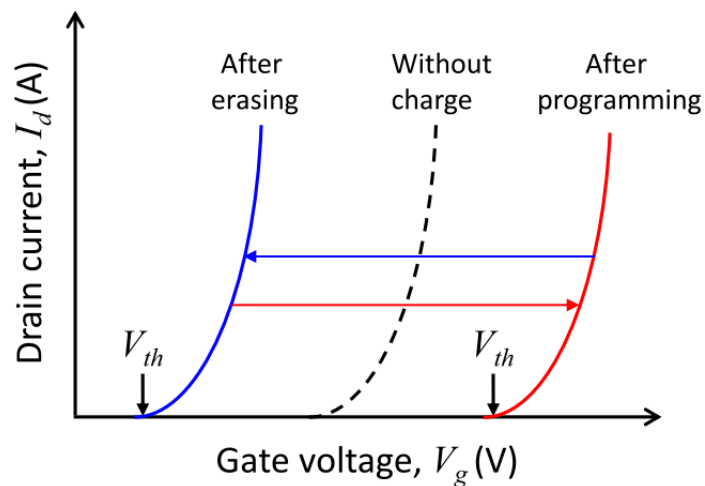
Fig. 1.2 I_d-V_g characteristics of the MONOS-type memory transistor in programming and erasing operations.

operations which are currently being employed in commercially available NVMs. Channel hot electron (CHE) injection is the popular programming mechanism. The minority carriers that flow in the channel of a memory transistor are accelerated by the high electric field generated by a large drain bias. Some of minority carriers gain sufficient kinetic energy to overcome the energy barrier at the tunnel oxide-silicon substrate interface, and are injected into the silicon nitride charge trapping film. From the point of view of the memory cell operation, the CHE injection mechanism gives high programming speed. However, a high drain current is needed to conduct the programming operation, resulting in high power consumption.

On the other hand, programming and erasing operations can be also achieved by the quantum mechanical tunneling of electrons and holes through the tunnel oxide film from the silicon substrate to the silicon nitride film. Figure 1.3(a) shows an n-channel MONOS-type memory transistor in the programming operation. When a sufficiently high positive voltage is applied to the gate electrode with grounded silicon substrate, a surface inversion
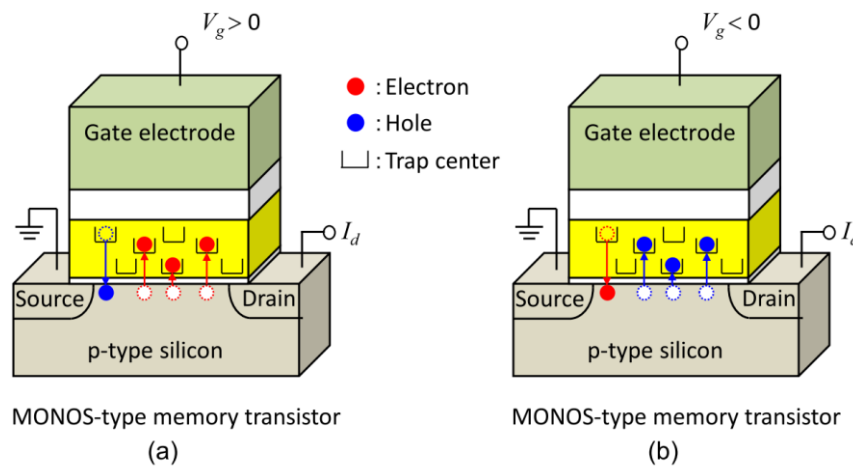
Fig. 1.3 MONOS-type memory transistors in: (a) programming operation and (b) erasing operation.

layer is formed between the source and drain. Some of electrons generated in the surface inversion layer are injected through the tunnel oxide film to the silicon nitride film and holes are eliminated from trap centers simultaneously. Figure 1.4(a) illustrates the energy band diagram of the gate electrode-blocking oxide-silicon nitride-tunnel oxide-silicon structure. The energy barrier for electron tunneling from the conduction band of silicon to the conduction band of silicon nitride becomes small enough due to the applied voltage across the structure. To obtain a high tunneling probability of electrons, the thickness of the tunnel oxide film is selected to be thinner than 3nm. Figure 1.3(b) shows the MONOS-type memory transistor in the erasing operation. Holes are injected through the thin tunnel oxide film from the silicon substrate to the silicon nitride film under a negative gate bias and electrons are eliminated from trap centers simultaneously. As shown in Fig. 1.4(b), holes tunnel from the valence band of silicon to the valence band of silicon nitride. The tunnel oxide thickness is required to be thinner than 3 nm to achieve sufficient erasing
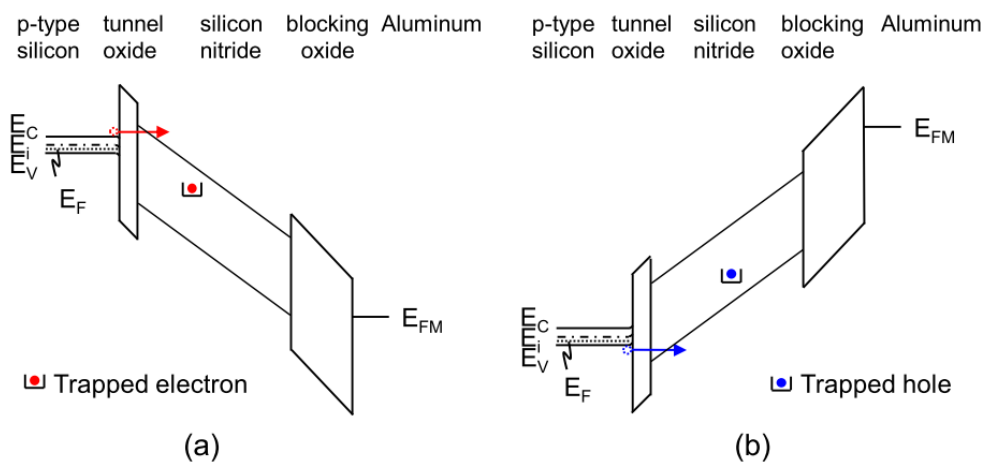
Fig. 1.4 Energy band diagrams of MONOS-type structures in: (a) programming operation and (b) erasing operation. At positive and negative gate biases, electrons and holes are injected through the thin tunnel oxide film from the silicon substrates to the silicon nitride films.

speed at a low gate voltage. With this injection mechanism, almost charge carriers injected to the silicon nitride film at low gate voltages are captured by charge trap centers existing in the silicon nitride film. This mechanism provides low power consumption, which is a consequence of a high ratio of the number of trapped carriers to that of injected carriers. Therefore, the MONOS-type memory devices with the thin tunnel oxide film thinner than 3 nm have attracted much attention for embedded NVM applications [9,10].

1.2   Requirements for nonvolatile memories

High programming and erasing speeds, long data retention time and good write endurance are important features of NVMs. The typical data retention time required in embedded NVMs is longer than 10 years [3,9,10]. The write endurance means the number of programming and erasing cycles before degradation of NVMs. Typically, the number of endurance cycles is 10^3 to 10^5 [3,9,10].

In the last few decades, the memory cell size has been becoming smaller in order to meet requirements of high capacity and low cost. As a result, the number of electrons and holes trapped in the silicon nitride film was reduced in such small size cells. Therefore, it is a challenge to promote the programming and erasing speeds and data retention in MONOS-type memories simultaneously. To overcome the challenge, many efforts have been expended in exploring new dielectric materials with superior properties [12-17]. However, no previous studies have been successful in replacing the silicon nitride film because of insufficient charge trapping characteristics provided by the materials.

As mentioned in section 1.1, electrons and holes captured by charge trap centers distributed in the silicon nitride film induce a shift in the threshold voltage of MONOS-type memory transistors, which are applied to store data. The presence of the charge trap centers in the silicon nitride films are responsible for the charge storage in MONOS-type memories. The properties of electron and hole trap centers in the silicon nitride films, such as, spatial distribution, density, capture cross section and energy level in the band gap influence the performance and reliability of MONOS-type memories. Specifically, the programming and erasing speeds depend on the density and capture cross section of electron and hole trap centers. The data retention mainly depends on the spatial distribution and energy level of trap centers. Consequently, the understanding of the

properties of electron and hole trap centers is important to achieve the better charge trapping characteristics of MONOS-type memories.

In the previous studies on silicon nitride films, it has been suggested that several kinds of point defects, such as the silicon dangling bond ($\cdot Si \equiv N_3$), nitrogen dangling bond, hydrogen-incorporated nitrogen vacancy, oxygen-incorporated nitrogen vacancy and so on, can be origins of electron and hole trap centers [18-28]. On the other hand, recent studies using electron spin resonance (ESR) have shown that silicon dangling bonds exist in high density in silicon carbonitride (denoted as SiCN in this dissertation) dielectric films grown using a plasma-enhanced chemical vapor deposition (PECVD) technique [29-31]. The elemental compositions of the SiCN films obtained using X-ray photoelectron spectroscopy measurements are presented in chapter 2. The density of the silicon dangling bonds was estimated to be 2×10^{19} cm^{-3}, which was roughly equal to that of silicon nitride films grown using a low-pressure chemical vapor deposition (LPCVD) method. Therefore, it was expected that charge trap centers are present in high density in the SiCN films, and then the application of SiCN films to the charge trapping films was intensively studied by Naito *et al.* [32] and Kobayashi *et al.* [33]. In these previous studies, it was found that the SiCN-based memory, in which the silicon nitride charge trapping film was replaced to the SiCN film, has higher programming and erasing speeds than that of the silicon nitride-based memory [32,33].

The energy band gap of the SiCN films is 3.4-3.8 eV, which is narrower than that of the silicon nitride films (~5 eV). Figure 1.5(a) shows the energy band diagram of the aluminum-blocking oxide-SiCN-tunnel oxide-silicon structure. At a large negative gate voltage, holes are injected from the valence band of silicon to the valence band of SiCN.
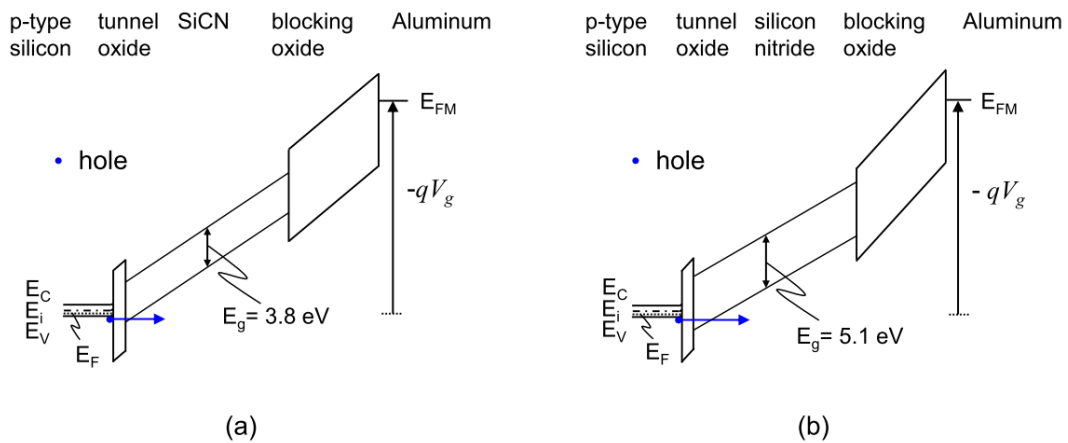
Fig. 1.5 (a) Energy band diagram of the aluminum-blocking oxide-SiCN-tunnel oxide-silicon structure at negative gate voltage. (b) Energy band diagram of the aluminum-blocking oxide-silicon nitride-tunnel oxide-silicon structure at negative gate voltage. The narrow energy band gap of the SiCN films would reduce the energy barrier for carrier injection to the SiCN charge trapping film from the silicon substrate.

An energy barrier for tunneling of holes is present between the valence bands of silicon and SiCN. Figure 1.5(b) shows the energy band diagram of the aluminum-blocking oxide-silicon nitride-tunnel oxide-silicon structure. As shown in Figs. 1.5(a) and 1.5(b), it is expected that the narrow energy band gap of the SiCN film gives a small energy barrier for the carrier injection from the silicon substrate to the SiCN charge trapping film. Moreover, the relative dielectric constant of SiCN films is 4.8-4.9, which is remarkably low as compared to that of silicon nitride films (~7). The density of carriers trapped in the charge trapping film which would be necessary to induce a fixed threshold voltage shift is a function of the dielectric constant of the charge trapping film. Therefore, the necessary carrier density in the low-dielectric constant SiCN charge trapping film is low as compared to that in the silicon nitride charge trapping film. These would result in high programming and erasing speeds and low power consumption in the SiCN-based memory. Unfortunately, there are few reports on the charge trapping characteristics of the SiCN-

based memory. Further study on the charge trapping phenomena is required to understand the mechanisms of programming and erasing operations in the SiCN-based memories.

As was mentioned above, the properties of charge trap centers affect the programming and erasing speeds and the data retention of NVMs. Therefore, a better understanding of the electron and hole trapping mechanisms and of the emission mechanism of trapped carriers in the charge trapping films is important. The carrier trapping and elimination mechanisms involved in the programming and erasing operations are listed in Fig. 1.6. The programming operation is caused by the electron trapping and hole elimination, as shown in Fig. 1.6. On the other hand, the hole trapping and electron elimination are responsible for the erasing operation. The probability of hole tunneling from the silicon

■ **Programming operation**

☐ Electron trapping
  ➢ Probability of electron tunneling
    from silicon to charge trapping films
  ➢ Properties of electron trap centers
    • Capture cross section
    • Density
    • Spatial distribution

☐ Hole elimination
  ➢ Probability of hole tunneling
    from charge trapping films to silicon
  ➢ Properties of hole trap centers
    • Density
    • Spatial distribution

■ **Erasing operation**

☐ Hole trapping
  ➢ Probability of hole tunneling
    from silicon to charge trapping films
  ➢ Properties of hole trap centers
    • Capture cross section
    • Density
    • Spatial distribution

☐ Electron elimination
  ➢ Probability of electron tunneling
    from charge trapping films to silicon
  ➢ Properties of electron trap centers
    • Density
    • Spatial distribution

Fig. 1.6 Carrier trapping and elimination mechanisms involved in programming and erasing operations.

substrate to the charge trapping film and the properties of hole trap centers such as capture cross section, density and spatial distribution affect the hole trapping in the erasing operation. Additionally, the electron elimination is influenced by the probability of electron tunneling from the charge trapping film to the silicon substrate and the properties of electron trap centers such as density and spatial distribution. In the present study, to get a better understanding of the mechanisms of programming and erasing operation, the constant-current carrier injection method was proposed. The hole trapping phenomenon in the SiCN charge trapping films was investigated by using the proposed constant-current carrier injection method. The electron elimination phenomenon of the SiCN charge trapping films in the erasing operation was also investigated by using the proposed method.

In addition, the data retention time is of concern for NVMs. Figure 1.7 shows the carrier emission mechanisms involved in the data retention. At low temperatures, the quantum mechanical tunneling dominates carrier emission from the charge trapping film to the silicon substrate. On the other hand, the thermal emission of trapped carriers is the

■ **Data retention**

    ❑ Electron retention   ❑ Hole retention

        ➢ Low temperature   ➢ Low temperature

            ● Tunnel emission   ● Tunnel emission

               ◆ Energy level   ◆ Energy level

        ➢ High temperature   ➢ High temperature

            ● Thermal emission   ● Thermal emission

               ◆ Energy level   ◆ Energy level

Fig. 1.7 Carrier emission mechanisms involved in data retention.

dominant mechanism at high temperatures. The energy level of trap centers in the band gap of charge trapping films affects the data retention characteristics at both low and high temperatures. Therefore, the understanding of the energy distribution of carriers trapped in the charge trapping films is essential to achieve the sufficient data retention characteristics of NVMs. To estimate the energy distribution of carriers trapped in the band gap of dielectric materials, an analysis method is required. In this study, an improved analytical method for the charge retention characteristics was presented to obtain the energy distribution of carriers trapped in the charge trapping films.

In the following section 1.3, problems in the current available methods for analyzing the charge trapping characteristics were discussed. In addition, problems of the analytical retention models, reported in the previous studies for obtaining the energy distribution of electrons trapped in the silicon nitride films, were also described.

1.3 Problem statement and research objectives

Analysis of charge trapping phenomena

In the previous studies, the charge centroid of holes trapped in the silicon nitride films of MONOS-type devices in programming condition was extracted by using the constant-voltage carrier injection method [2,34-43]. However, the constant-voltage carrier injection method required the application of an auxiliary pulse [34,39], which might cause an error in the charge centroid estimation. In this dissertation, the constant-current carrier injection method was proposed to analyze the charge centroid of carriers trapped in the charge trapping films and to count the number of carriers injected to the films. The proposed method does not require the application of the auxiliary pulse before carrier injection. Therefore, the proposed constant-current carrier injection method is useful for obtaining the accurate charge centroid of carriers trapped in the charge trapping films.

As was explained in section 1.1, the MONOS-type devices can store information by capturing electrons and holes by trap centers distributed in silicon nitride charge trapping films. There are three states of the charge trap centers: (i) empty trap centers, (ii) trap centers filled by electrons, and (iii) trap centers filled by holes. In the previous studies, several researchers have evaluated the charge centroid of holes trapped in the silicon nitride films during the erasing operation subsequent to the programming operation [2,34-43]. During the programming operation, trap centers filled by electrons ought to be generated in the films due to electron injection into the silicon nitride films. In the erasing operation subsequent to the programming operation, holes are injected into the charge trapping film and are captured by trap centers. Simultaneously, electrons captured by trap centers during the programming operation are emitted from the charge trapping film. The charge centroid obtained in the previous works would result from the spatial distribution

of the electrons captured by trap centers in addition to the distribution of the holes captured by trap centers in the charge trapping films. Therefore, it was difficult to clarify the accurate location of holes trapped in the charge trapping films. On the other hand, in this study, the charge centroid of holes captured by empty trap centers in the charge trapping films without trapped electrons was investigated by using the proposed constant-current carrier injection method.

As mentioned in section 1.2, recently, the SiCN dielectric film has been expected to be an attractive candidate of the charge trapping film of embedded NVMs instead of the silicon nitride film. Unfortunately, there are few reports on the charge trapping phenomenon in the SiCN-based memory. To get a better understanding of the mechanisms of erasing operation, the charge centroid of holes trapped in the SiCN and silicon nitride charge trapping films with only empty trap centers was evaluated by using the proposed constant-current carrier injection method.

In addition, the elimination of electrons trapped in the SiCN and silicon nitride charge trapping films during erasing operation was studied by using the proposed method.

Analysis of the energy distribution of trapped electrons

The charge retention characteristics is one of the important features of NVMs. As was mentioned in section 1.2, the charge retention time of NVMs depends on the energy level of carriers trapped in the charge trapping films.

In the previous studies for MONOS-type devices, several researchers have reported analytical retention models based on the direct tunneling, trap-to-band tunneling and thermal excitation of electrons to derive the energy distribution of electrons trapped in silicon nitride charge trapping films. To determine the energy distribution of trapped

electrons, a set of adjustable and assumed parameters, such as mean free path for the direct tunnelling of electrons, inverse of the attempt-to-escape frequency for thermal excitation and trap capture cross section of silicon nitride films, were needed in the previous models [8,44-46]. Moreover, additional sets of other experiments were required to determine these parameters.

Unfortunately, there has been no report concerning the appropriate values of these parameters for new dielectric films. Consequently, a new method is required to derive the energy distribution of electrons trapped in the new dielectric films. In this work, an improved analytical method for the charge retention characteristics in the charge trapping films was presented. This method allows us to extract the energy distribution of carriers trapped in new dielectric films without using any adjustable parameters.

To date, the energy level of trap centers in the SiCN charge trapping films has never been analyzed. In this dissertation, the energy distribution of electrons trapped in the SiCN films was obtained by using the proposed method without using any adjustable parameters.

1.4　Organization of dissertation

This dissertation consists of five chapters. The contents of each chapter are briefly described as follows.

Chapter 1　In this chapter, the structure and programming and erasing operations of MONOS-type memory devices are firstly introduced. Next, a brief explanation of the requirements for NVMs is given. The influence of the properties of charge trap centers on the performance and reliability of NVMs is briefly mentioned also. The background and objectives of the present research is presented.

Chapter 2　In this chapter, the constant-current carrier injection method is proposed to obtain the charge centroid of charge carriers trapped in the charge trapping films and to count the number of carriers injected to the films. The proposed method is used to inject holes into the SiCN and silicon nitride charge trapping films with only empty trap centers, and the charge centroid of holes trapped in the films is extracted. The background of the research objectives of this chapter would be introduced firstly. Then, the formation conditions of samples employed in this chapter are given. In order to investigate the elemental compositions in the blocking oxide-SiCN-tunnel oxide and the blocking oxide-silicon nitride-tunnel oxide stacked films, X-ray photoelectron spectroscopy (XPS) measurements are performed. Next, atomic force microscopy (AFM) is used to investigate the surface roughness of the SiCN, silicon nitride, blocking oxide, and tunnel oxide single-layer films. In this chapter, the extraction method of the charge centroid of trapped carriers in memory capacitors subjected to the constant-current carrier injection will be explained in detail. The leakage current in the stacked dielectric films is also

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analyzed. Then, the experimental results of the charge centroid of holes trapped in the SiCN and silicon nitride films after constant-current hole injection are presented. In addition, the variations of the charge centroid of holes captured by only empty trap centers in the SiCN and silicon nitride films is explained by taking into account the Poole-Frenkel (PF) conduction of holes in the films. Finally, the conclusions of this chapter are provided.

Chapter 3   This chapter focuses on the investigation of the electron elimination phenomena in the SiCN and silicon nitride charge trapping films with trap centers filled by electrons using the constant-current carrier injection method. First, measurement procedures of the hole trapping characteristics of two conditions are given. Then, the flat-band voltage shift in the memory capacitors with trap centers filled by electrons and only empty trap centers is described using the capacitance-voltage (CV) characteristics under negative gate bias. The constant-current carrier injection method presented in chapter 2 is used to count the number of holes injected to the charge trapping films with both trap centers filled by electrons and empty trap centers. Finally, the electron elimination in the erasing operation of the SiCN and silicon nitride memory capacitors is discussed.

Chapter 4   In this chapter, an improved analytical method for the charge retention characteristics is presented to obtain the energy distribution of electrons trapped in the charge trapping films. This method allows the extraction of energy level of electrons trapped in the SiCN or new dielectric films without using any adjustable parameters. Firstly, the background of the research objectives of this chapter is introduced. The experimental procedures for measuring the charge retention characteristics of memory capacitors is described. Then, the procedure of the flat-band voltage determination by analyzing the CV characteristics during the charge retention test is shown. The charge

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retention characteristics of the SiCN memory capacitors at 86 °C is presented. To analyze the energy distribution of electrons trapped in the SiCN films, the charge retention characteristics in the programming condition are measured at four different temperatures. Then, the improved analytical method for the charge retention characteristics based on thermal excitation mechanism is discussed. In this chapter, the trapped electrons are determined to be distributed from 0.8 to 1.3 eV below the conduction band edge in the SiCN charge trapping film.

Chapter 5   This chapter summarizes the dissertation work, and finally makes suggestions for future studies.

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Chapter 2

Investigation of hole trapping characteristics in SiCN charge trapping films using the constant-current carrier injection method

Chapter 2　Investigation of hole trapping characteristics in SiCN charge trapping films using the constant-current carrier injection method

2.1　Introduction

As described in chapter 1, the metal-oxide-nitride-oxide-silicon (MONOS)-type charge trapping memory with an ultrathin tunnel oxide film thinner than 3 nm has received significant attention as an attractive solution for embedded nonvolatile memory (NVM) applications [1-10]. This is because the MONOS-type memory devices furnish several advantages such as low programming and erasing voltages, ease of integration into a standard complementary metal-oxide-semiconductor (CMOS) process flow, and excellent scalability. In the MONOS-type devices, electrons and holes are injected into the silicon nitride charge trapping film via the quantum mechanical tunneling and are captured by charge trap centers existing in the nitride film. The electrons and holes trapped in the silicon nitride film induce a shift in the threshold voltage of memory transistors. This phenomenon is applied to programming and erasing operations in the MONOS-type memory cells. In the past few decades, the amount of charge stored in the charge trapping film has been decreasing because of shrinkage of the memory cell size in the MONOS-type devices. Therefore, there are still some challenges to obtain the excellent performance and reliability in the MONOS-type devices. Accordingly, many researchers have intensively explored new dielectric materials with the superior charge trapping characteristics [11-16]. However, no previous studies have been successful in replacing the silicon nitride film because of insufficient charge trapping characteristics provided by the new materials.

As mentioned in section 1.2 in chapter 1, the application of SiCN films to the charge trapping film of the embedded NVMs was intensively studied by Naito *et al*. [17] and Kobayashi *et al*. [17,18]. In addition, it was found that the SiCN-based memory has higher programming and erasing speeds than that of the silicon nitride-based memory [17,18]. However, the understanding of the charge trapping phenomena in the programming and erasing operations is still important to realize the SiCN-based NVMs.

There are three states of the charge trap centers: (i) empty trap centers, (ii) trap centers filled by electrons, and (iii) trap centers filled by holes. Several studies have been made on the hole trapping characteristics of the silicon nitride-based charge trapping memory after electron injection [2,19-29], in which the charge centroid of holes trapped in the silicon nitride films with trap centers filled by electrons has been investigated by using the constant-voltage carrier injection method. Both empty trap centers and trap centers filled by electrons ought to exist in the silicon nitride films after the programming operation. Holes injected to the silicon nitride films would be captured by both two states of the trap centers. The charge centroid obtained in the previous studies would result from hole capture by both empty trap centers and trap centers filled by electrons. Moreover, during hole injection, both electrons and holes captured by trap centers would be present in the silicon nitride films. The electrons could be moved inside the films and could be emitted from the silicon nitride films. Therefore, it is difficult to clarify the accurate location of trapped holes.

In this chapter, to get a better understanding of the mechanisms of erasing operation, the constant-current carrier injection method was proposed and the charge centroid of holes trapped in the SiCN and silicon nitride charge trapping films with only empty trap centers was extracted.

In the previous studies, the constant-voltage carrier injection method was used to evaluate the charge centroid in the silicon nitride-based charge trapping memory [19,24]. This method required the application of an auxiliary pulse before carrier injection. By applying the auxiliary pulse, the silicon surface potential is returned to flat-band condition. However, to determine the auxiliary pulse level, another set of measurements of programming and erasing characteristics is needed in preliminary step. Such a sequence would generate an error in the charge centroid estimation due to the variation of the programming and erasing characteristics among individual memory transistors. On the other hand, in the present study, the proposed constant-current carrier injection method does not require the additional measurement of the programming and erasing characteristics and the application of the auxiliary pulse. The constant-current carrier injection method is useful to obtain the accurate charge centroid of carriers trapped in the charge trapping films. In this chapter, a comparative study of the charge centroid of holes captured by empty trap centers in the SiCN and silicon nitride charge trapping films was made using the proposed constant-current hole injection method.

This chapter is organized as follows. In section 2.2, the formation conditions of films, the elemental compositions throughout the film thickness and surface roughness of the fabricated films will be presented. Then, the experimental procedure for measuring the hole trapping characteristics will be described. In section 2.3, an extraction method of the charge centroid of trapped carriers will be discussed. After that, the leakage current through the stacked dielectric films will be analyzed. Then, the experimental results of the charge centroid of holes trapped in the charge trapping films will be presented. The distribution of holes trapped in the SiCN and silicon nitride films around the charge centroid will be explained by a model. Finally, section 2.4 provides the conclusions.

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2.2　Experimental details

2.2.1 Films fabrication

Two types of memory capacitors with blocking oxide-SiCN-tunnel oxide and blocking oxide-silicon nitride-tunnel oxide stacked films were formed on p-type (100) silicon substrates. The schematic cross sections of the fabricated memory capacitors are shown in Fig. 2.1. The formation conditions of the samples are summarized in Table 2.1. A tunnel oxide film of 2.4 nm in thickness was formed by rapid thermal oxidation at 1050 °C of the silicon substrates in both types of the stacked dielectric films. A 31.6-nm-thick SiCN film was formed by a PECVD technique at 400 °C using $Si(CH_3)_4$ and NH_3 gases. A 30.4-nm-thick silicon nitride film was grown at 600 °C using Si_2Cl_6 and NH_3 gases by an LPCVD technique. A blocking oxide film of 17.2-17.3 nm in thickness was formed by a PECVD technique at 400 °C using SiH_4 and N_2O gases. Finally, an aluminum film was deposited by thermal evaporation through a metal mask (shadow mask evaporation) to form the gate electrode. The aluminum gate electrode can be formed without damage by this technique. The refractive indexes of the SiCN and silicon nitride films were found to be 1.91 and 1.97 at a wavelength of 632.8 nm using a SOPRA MOSS-ES4G spectroscopic ellipsometer. The static relative dielectric constant of the SiCN and silicon nitride films were estimated to be 4.8 and 7.3, respectively.
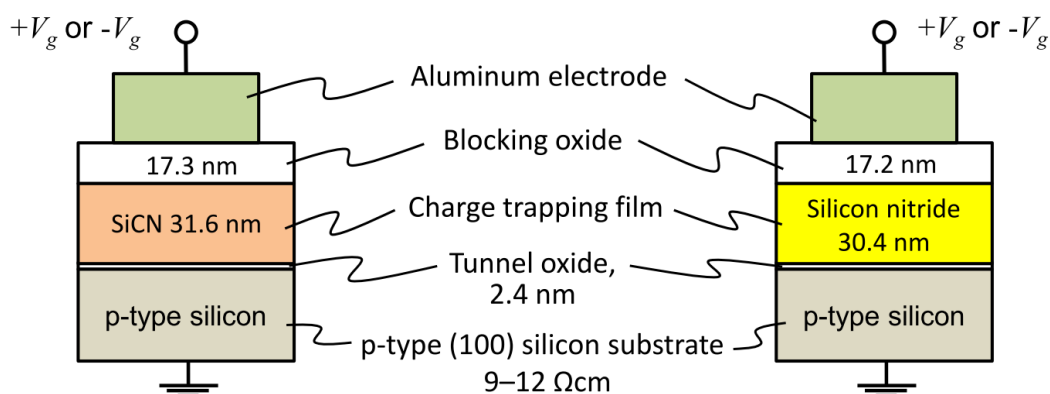
Fig. 2.1 Schematic cross sections of the memory capacitors with an aluminum electrode-blocking oxide-SiCN-tunnel oxide-silicon and an aluminum electrode-blocking oxide-silicon nitride-tunnel oxide-silicon. Figure 2.1 is "Reproduced with permission from ECS Transactions, 75(32), 51 (2017). Copyright 2017, The Electrochemical Society."

Table 2.1 Summary of the formation conditions of the samples.

Film	Thickness (nm)	Refractive index	Method	Temperature (°C)	Source gases
Blocking oxide	17.2-17.3	1.48	PECVD	400	SiH_4+N_2O
SiCN	31.6	1.91	PECVD	400	$Si(CH_3)_4+NH_3$
Silicon nitride	30.4	1.97	LPCVD	600	$Si_2Cl_6+NH_3$
Tunnel oxide	2.4	1.46	Thermal oxidation	1050	

2.2.2 Elemental compositions and surface roughness of fabricated films

In order to investigate elemental compositions of the stacked films, X-ray photoelectron spectroscopy (XPS) measurements were performed using an ULVAC-PHI Quantum 2000 spectrometer with a monochromatic Al Kα (1486.6 eV) X-ray source. The XPS spectra were collected for carbon (C 1s), nitrogen (N 1s), oxygen (O 1s), and silicon (Si 2p) elements after every 1-min sputtering by using a 1 kV Ar ion beam sputtering. The diameter of the X-ray beam area was 50 μm and the detection system was located at 45° with respect to the surface of the samples. Figures 2.2(a) and 2.2(b) show the XPS depth profiles of the blocking oxide-SiCN-tunnel oxide and the blocking oxide-silicon nitride-tunnel oxide stacked films fabricated on p-type silicon substrates. The XPS depth profiles represent the relationships between the Ar ion sputtering time and the atomic ratios. The atomic ratios were calculated from atomic concentrations of the elements, in which the atomic concentrations of the elements were derived from the corresponding photoelectron peak areas. Table 2.2 shows the summary of depth profiles of the atomic ratios. In Table 2.2, the mean atomic ratios of N, C, and O to Si were given. The mean atomic ratio of O to Si in the blocking oxide films was estimated within the 1 to 5 min sputtering time range. Additionally, within the 14 to 26 min sputtering time range in Figs. 2.2(a) and 2.2(b), the mean atomic ratios of N and C to Si in the SiCN and silicon nitride films were calculated. The errors shown in Table 2.2 are single standard deviation. It was found that the atomic ratios of N, C, and O to Si were nearly constant throughout the thickness of the blocking oxide, SiCN, and silicon nitride films.
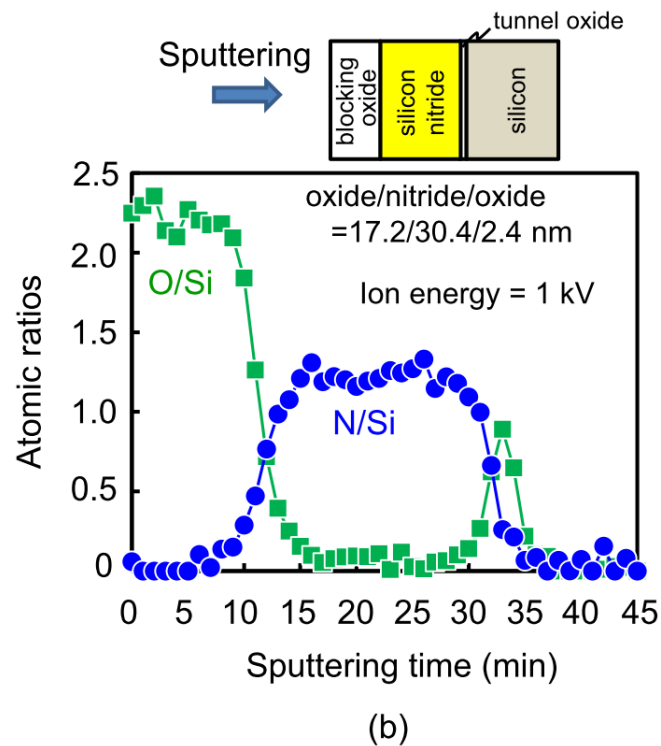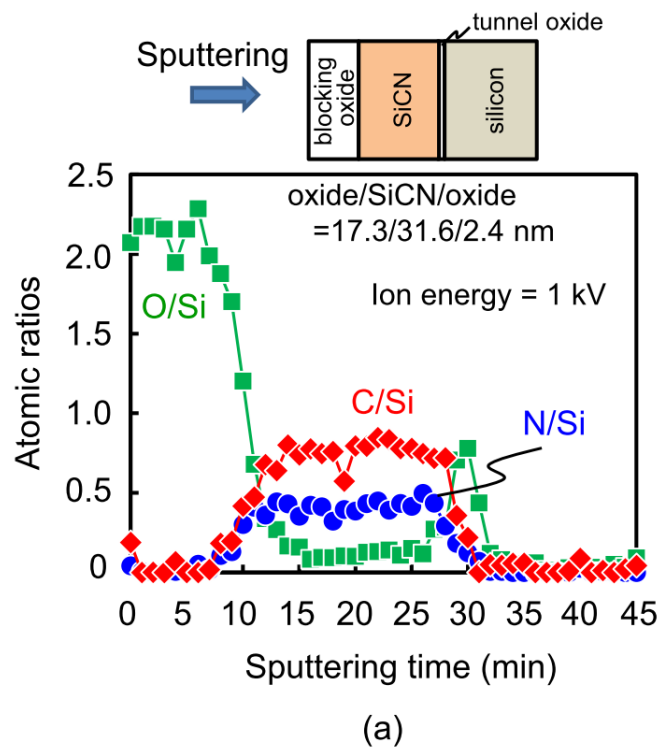
Fig. 2.2 (a) XPS depth profiles of the blocking oxide-SiCN-tunnel oxide stacked films fabricated on p-type silicon substrate. (b) XPS depth profiles of the blocking oxide-silicon nitride-tunnel oxide stacked films fabricated on p-type silicon substrate.

Table 2.2 Summary of the depth profiles of the atomic ratios in the blocking oxide, SiCN, and silicon nitride films. This Table is "Reprinted from Materials Science in Semiconductor Processing, 2017, in press, S. R. Al Ahmed, K. Kato, and K. Kobayashi, Hole trapping characteristics of silicon carbonitride (SiCN)-based charge trapping memories evaluated by the constant-current carrier injection method, Copyright (2017), with permission from Elsevier."

Atomic ratio	Blocking oxide	SiCN	Silicon nitride
N/Si	-	0.41 ± 0.04	1.22 ± 0.06
C/Si	-	0.77 ± 0.06	
O/Si	2.10 ± 0.11	-	-

Next, the surface roughness of the SiCN, silicon nitride, blocking oxide, and tunnel oxide single-layer films was investigated by atomic force microscopy (AFM) technique. A Shimadzu SPM-9700 AFM system with a scan size of 1.0 μm × 1.0 μm in tapping mode configuration was used to measure the surface roughness of the films. Figures 2.3(a), 2.3(b), 2.3(c), and 2.3(d) show the three-dimensional AFM images of the SiCN, silicon nitride, blocking oxide, and tunnel oxide films. The surface roughness of the films was characterized by most commonly used roughness parameters such as the arithmetic mean roughness (R_a) and root-mean-square roughness (R_q). Table 2.3 summarizes R_a and R_q obtained from AFM analysis. It was found that the surface of the fabricated films was smooth with the small roughness values of R_a and R_q.

(a) SiCN, 31.6 nm

(b) Silicon nitride, 30.4 nm

(c) Blocking oxide, 17.2-17.3 nm
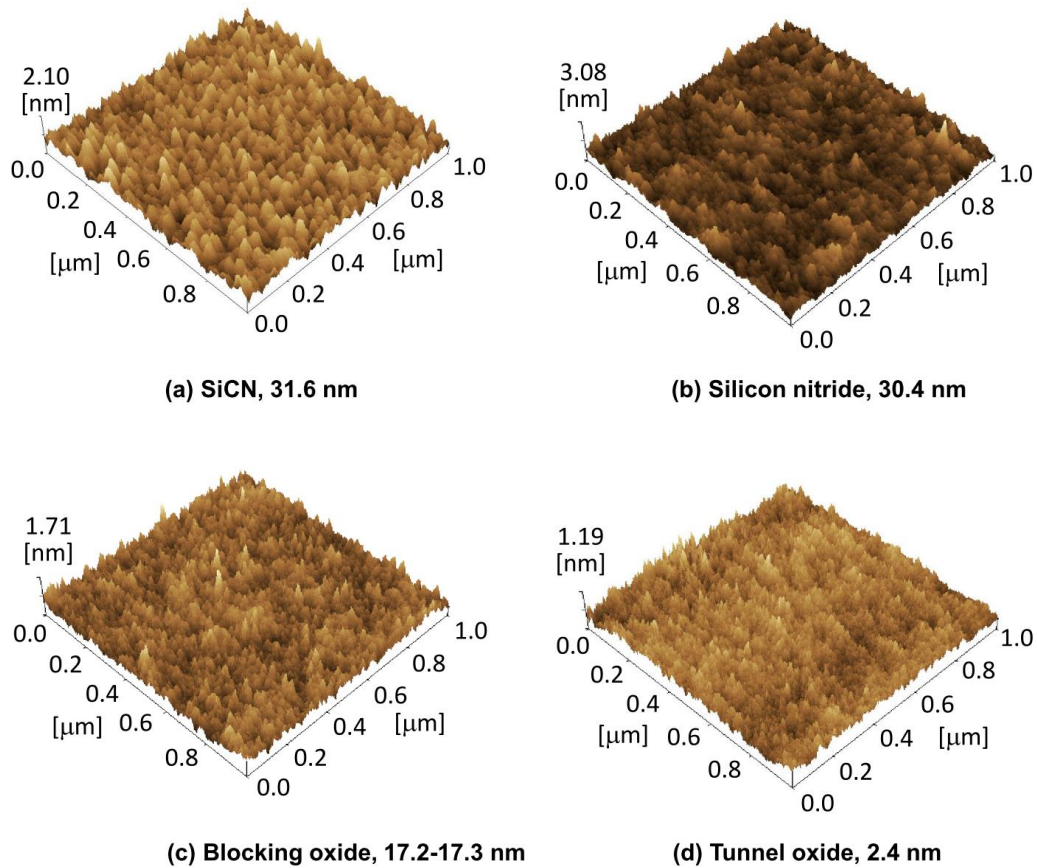
(d) Tunnel oxide, 2.4 nm

Fig. 2.3 Three-dimensional AFM images of four different single-layer films: (a) SiCN film of 31.6 nm in thickness, (b) silicon nitride film of 30.4 nm in thickness, (c) blocking oxide film of 17.2-17.3 nm in thickness, and (d) tunnel oxide film of 2.4 nm in thickness.

Table 2.3 Summary of the surface roughness of the SiCN, silicon nitride, blocking oxide, and tunnel oxide films. Table 2.3 is "Reprinted from Materials Science in Semiconductor Processing, 2017, in press, S. R. Al Ahmed, K. Kato, and K. Kobayashi, Hole trapping characteristics of silicon carbonitride (SiCN)-based charge trapping memories evaluated by the constant-current carrier injection method, Copyright (2017), with permission from Elsevier."

Film	Thickness (nm)	Arithmetic mean roughness, R_a (nm)	Root-mean-square roughness, R_q (nm)
SiCN	31.6	0.20	0.25
Silicon nitride	30.4	0.19	0.25
Blocking oxide	17.2-17.3	0.14	0.17
Tunnel oxide	2.4	0.11	0.12

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2.2.3 Procedures for measuring hole trapping characteristics

Figure 2.4 shows the experimental procedure for measuring the hole trapping characteristics. After sample fabrication, all the memory capacitors were baked at 235 °C for a long period of time to emit electrons and holes trapped in the blocking oxide-SiCN-tunnel oxide and the blocking oxide-silicon nitride-tunnel oxide stacked films. The high-frequency capacitance-voltage (CV) measurements were conducted and the flat-band voltage $V_{fb,0}$ was determined by analyzing the CV curves of the baked capacitors. The CV characteristics were measured at 100 kHz with an Agilent E4980A LCR meter. At the next step, the gate electrodes were negatively biased to inject holes from the silicon substrates into the charge trapping films at a constant current density of -4.2×10^{-9} A/cm^2. The constant-current hole injection was carried out using an Agilent 4157B semiconductor parameter analyzer. After the hole injection following the baking, the CV characteristics were again measured to determine the flat-band voltage $V_{fb,h1}$. Then, the flat-band voltage shift $\Delta V_{fb,h}$ was obtained from the difference between $V_{fb,0}$ and $V_{fb,h1}$. Next, the injected charge per unit area $Q_{inj}(t_0,t_1)$ was calculated by combining the current density J_g and carrier injection time. The charge centroid of trapped holes were estimated from $\Delta V_{fb,h}$ and $Q_{inj}(t_0,t_1)$. The detailed procedure to obtain the charge centroid of trapped holes is explained in section 2.3.1.

● Baking the sample capacitors at 235 °C
    Trapped carriers in the stacked films were emitted.

○ CV measurement (100 kHz)
    The flat-band voltage was determined: $V_{fb,0}$

● Constant-current hole injection at -4.2 × 10⁻⁹ A/cm²
    The gate was negatively biased to inject holes to the
    charge trapping film.

○ CV measurement (100 kHz)
    After hole injection, $V_{fb,h1}$ was measured to determine $\Delta V_{fb,h}$.

● ① The injected charge per unit area Q_{inj} was calculated.
  ② Charge centroid of trapped holes were estimated from $\Delta V_{fb,h}$ and Q_{inj}.

Fig. 2.4 Experimental procedure to extract the charge centroid of holes trapped in the charge trapping films using the constant-current hole injection method. This Figure is "Reproduced with permission from ECS Transactions, 75(32), 51 (2017). Copyright 2017, The Electrochemical Society."

The gate current density of -4.2 × 10⁻⁹ A/cm² was obtained from the gate current of -4.6 × 10⁻¹¹ A for the memory capacitors with an area of 1.1×10^{-2} cm² (1.1 mm²). The gate current below this level could not be employed by taking into consideration the noise level of the system used in this study (Agilent 4157B semiconductor parameter analyzer). In the case of injecting holes of 0.2×10^{13} cm⁻² in density, the constant gate current was kept for 250 s. If a gate current of -4.6 × 10⁻⁹ A is selected, hole injection should be conducted only for a period of 2.5 s. Since the highest time resolution of our system is 0.25 s, such a short period of time for hole injection is unsuitable to obtain an accurate number of injected holes.

2.3 Results and discussion

2.3.1 Extraction method of charge centroid of trapped holes

Figure 2.5(a) shows the CV characteristics of the SiCN capacitor after the baking at 235 °C and after the subsequent constant-current hole injection at -4.2×10^{-9} A/cm^2. The capacitor was first baked at 235 °C for a long period of time to empty all trap centers existing in the SiCN film. The 235 °C baking and the CV measurement were conducted alternately and it was confirmed that the flat-band voltage converged to a value of -3.4 V, which is termed as $V_{fb,0}$. Subsequently, holes were injected into the SiCN films with only empty trap centers from the silicon substrate through the thin tunnel oxide film via the quantum mechanical tunneling under the negative gate bias. After the hole injection, the flat-band voltage was shifted toward the negative voltage direction from $V_{fb,0}$ to $V_{fb,h1}$ due to holes captured by only empty trap centers in the SiCN charge trapping film. The flat-band voltage shift $\Delta V_{fb,h}$ was derived from the difference between $V_{fb,0}$ and $V_{fb,h1}$.

Figure 2.5(b) shows the CV characteristics of the silicon nitride capacitor after the baking at 235 °C and after the constant-current hole injection. The flat-band voltage $V_{fb,0}$ of the baked capacitor was determined to be -4.4 V for the silicon nitride capacitor. Subsequently, holes were injected into the silicon nitride film with only empty trap centers under the negative gate bias. $\Delta V_{fb,h}$ induced by holes trapped in the silicon nitride charge trapping film was obtained from the difference between $V_{fb,0}$ and $V_{fb,h1}$.
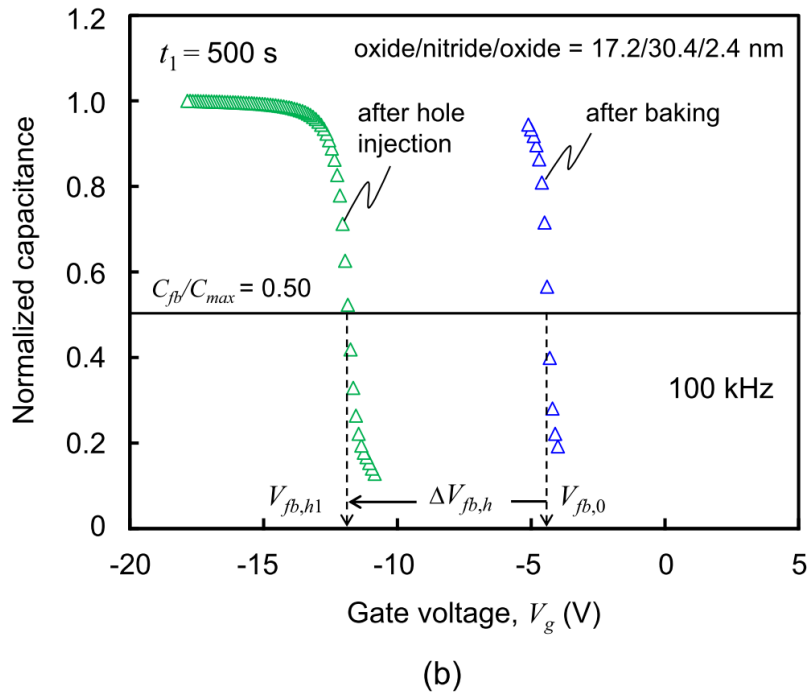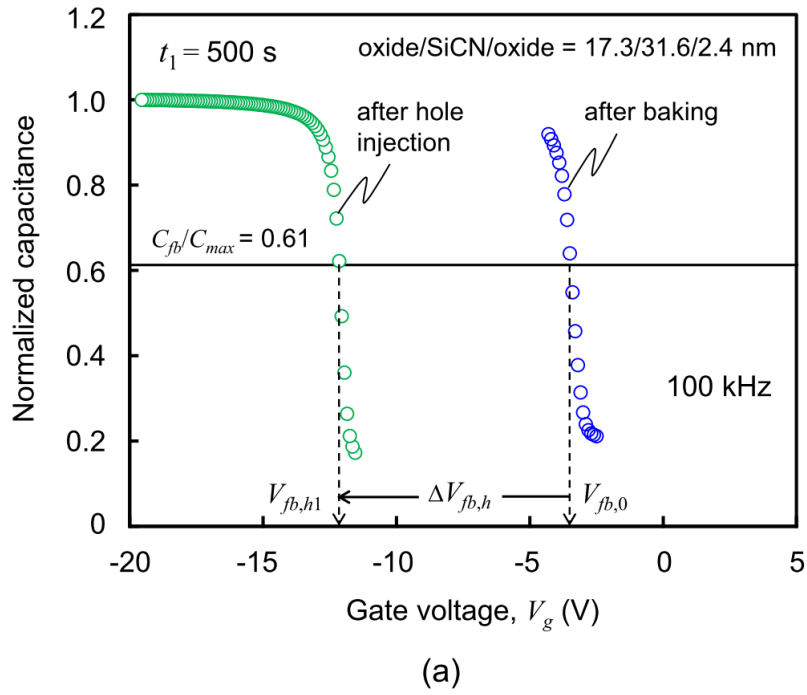
Fig. 2.5 (a) CV characteristics of the memory capacitor with the blocking oxide-SiCN-tunnel oxide stacked films. (b) CV characteristics of the memory capacitor with the blocking oxide-silicon nitride-tunnel oxide stacked films.

It is assumed that the trapped holes are distributed as a sheet of charge, which is located at the charge centroid $\bar{x}_{tctl}$. Here, $\bar{x}_{tctl}$ is measured from the interface between the blocking oxide and the charge trapping film, as shown in Fig. 2.6. The density of trapped charge Q_{trap} is given by

$$Q_{trap} = -\frac{1}{\dfrac{t_{box}}{\varepsilon_0\varepsilon_{box}} + \dfrac{\bar{x}_{tctl}}{\varepsilon_0\varepsilon_{ctl}}} \Delta V_{fb,h}, \tag{2.1}$$

where ε_{box} and ε_{ctl} are, respectively, the static relative dielectric constants of the blocking oxide and charge trapping films, t_{box} is the thickness of the blocking oxide film, ε_0
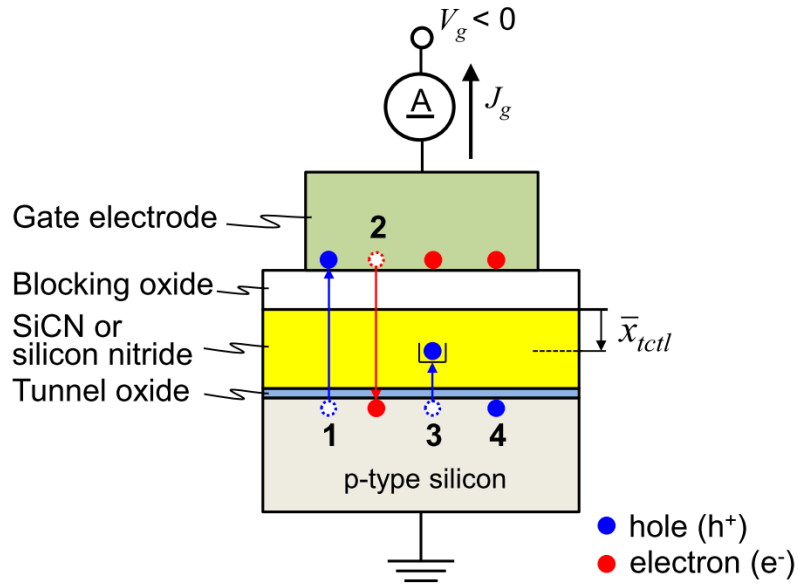
Fig. 2.6 Measurement configuration for extracting the charge centroid $\bar{x}_{tctl}$ of holes trapped in the SiCN and silicon nitride films. $\bar{x}_{tctl}$ was measured from the interface between the blocking oxide and the charge trapping films. The numbers 1 and 2 indicate the flows of holes and electrons across the stacked dielectric films, respectively. The number 3 indicates the hole capture by empty trap centers and 4 indicates the hole accumulation at the silicon surface.

is the permittivity of free space. Then, $\bar{x}_{tctl}$ is represented by [2,24,28,30]

$$\bar{x}_{tctl} = -\left(\frac{\Delta V_{fb,h}}{Q_{trap}} + \frac{t_{box}}{\varepsilon_0 \varepsilon_{box}}\right)\varepsilon_0 \varepsilon_{ctl} . \tag{2.2}$$

Figure 2.7(a) shows the gate voltage shift of the SiCN capacitor during the constant-current hole injection. The gate voltage shift of the silicon nitride capacitor during the hole injection is also shown in Fig. 2.7(b). Here, $Q_{meas}(t)$ is defined with the gate current density J_g and carrier injection time t by

$$Q_{meas}(t) = J_g \cdot t . \tag{2.3}$$

In Figs. 2.7(a) and 2.7(b), the gate voltage V_g increased with increasing $Q_{meas}(t)$. The silicon surface was under the inversion or depletion condition while V_g ranged from 0 to $V_{fb,0}$. When V_g was larger than $V_{fb,0}$, the silicon surface was in the accumulation condition and holes were injected from the silicon substrate into the charge trapping film through the thin tunnel oxide film via the quantum mechanical tunneling. $Q_{meas}'(t_0,t_1)$ is defined in the following formula

$$Q_{meas}'(t_0,t_1) = Q_{meas}(t_1) - Q_{meas}(t_0)$$
$$= J_g \cdot (t_1 - t_0) . \tag{2.4}$$

The gate current density J_g is written as

$$J_g = J_{leak}(t) + J_{trap}(t) + J_{sub}(t), \tag{2.5}$$

where $J_{leak}(t)$ is the leakage current component owing to electron and hole flows across the stacked dielectric films, $J_{trap}(t)$ is the displacement current component owing to hole trapping by trap centers existing in the charge trapping film and $J_{sub}(t)$
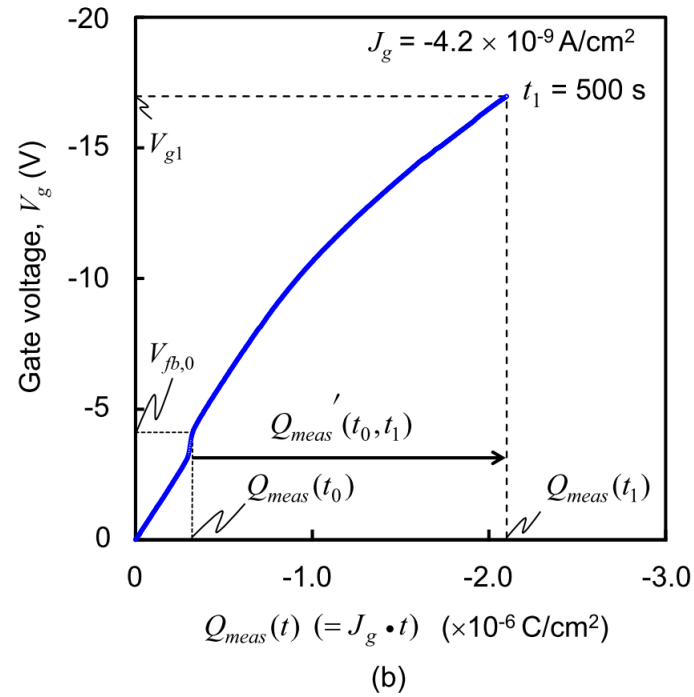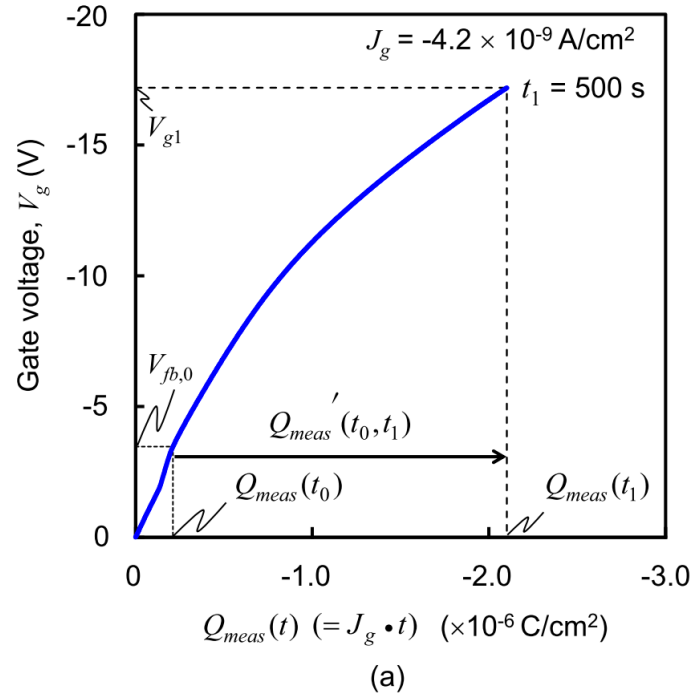
Fig 2.7 (a) Gate voltage shift as a function of $Q_{meas}(t)$ in the SiCN capacitor during the constant-current hole injection. (b) Gate voltage shift as a function of $Q_{meas}(t)$ in the silicon nitride capacitor during the hole injection. Figure 2.7(a) is "Reprinted from Materials Science in Semiconductor Processing, 2017, in press, S. R. Al Ahmed, K. Kato, and K. Kobayashi, Hole trapping characteristics of silicon carbonitride (SiCN)-based charge trapping memories evaluated by the constant-current carrier injection method, Copyright (2017), with permission from Elsevier."

is the displacement current component owing to hole accumulation at the silicon surface. Integration of Eq. (2.5) for the interval t_0 to t_1 in time yields

$$Q_{meas}{}'(t_0,t_1) = Q_{leak}(t_0,t_1) + Q_{trap}(t_0,t_1) + Q_{sub}(t_0,t_1).$$
(2.6)

Then, the injected charge per unit area $Q_{inj}(t_0,t_1)$ is defined by

$$Q_{inj}(t_0,t_1) \equiv Q_{leak}(t_0,t_1) + Q_{trap}(t_0,t_1) = Q_{meas}{}'(t_0,t_1) - Q_{sub}(t_0,t_1).$$
(2.7)

Here, $Q_{meas}{}'(t_0,t_1)$ can be determined by using Eq. (2.4) and $Q_{sub}(t_0,t_1)$ can be calculated by integrating the capacitance $C(V_g)$ of the memory capacitor after hole injection for the interval $V_{fb,h1}$ to V_{g1}

$$Q_{sub}(t_0,t_1) = \int_{V_{fb,h1}}^{V_{g1}} C(V_g)dV_g.$$
(2.8)

Therefore, $Q_{inj}(t_0,t_1)$ can be experimentally obtained from Eq. (2.7). If $Q_{leak}(t_0,t_1) = 0$, $Q_{trap}(t_0,t_1)$ is approximately given by

$$Q_{trap}(t_0,t_1) \cong Q_{inj}(t_0,t_1).$$
(2.9)

According to Eqs. (2.2) and (2.9), $\bar{x}_{tctl}$ is given by

$$\bar{x}_{tctl} = -\left(\frac{\Delta V_{fb,h}}{Q_{inj}(t_0,t_1)} + \frac{t_{box}}{\varepsilon_0 \varepsilon_{box}} \right) \varepsilon_0 \varepsilon_{ctl}.$$
(2.10)

2.3.2 Analysis of leakage current component

To estimate the $Q_{leak}(t_0, t_1)$ value, the leakage current component $J_{leak}(t)$ described in Eq. (2.5) was analyzed. Figure 2.8(a) shows the J_g-V_g characteristics of the blocking oxide-SiCN-tunnel oxide stacked films after the baking. At the first scan, the gate voltage was stepped by 0.1 V every 2 s (1 s of delay time before the measurement and 1 s for the current measurement) to avoid detecting the displacement current component owing to hole accumulation at the silicon surface. The presence of a large displacement current component was observed at gate voltages ranging from 0 to -18 V. This current component is mainly attributed to hole trapping by empty trap centers in the
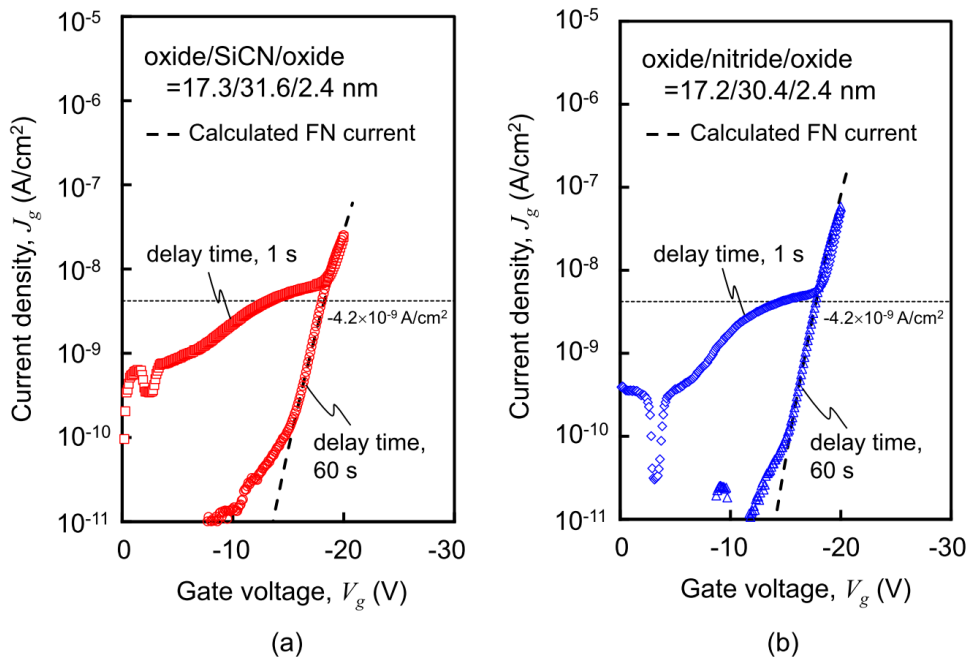
Fig. 2.8 (a) J_g-V_g characteristics of the memory capacitor with the blocking oxide-SiCN-tunnel oxide stacked films. (b) J_g-V_g characteristics of the memory capacitor with the blocking oxide-silicon nitride-tunnel oxide stacked films. Figures 2.8(a) and 2.8(b) are "Reprinted from Materials Science in Semiconductor Processing, 2017, in press, S. R. Al Ahmed, K. Kato, and K. Kobayashi, Hole trapping characteristics of silicon carbonitride (SiCN)-based charge trapping memories evaluated by the constant-current carrier injection method, Copyright (2017), with permission from Elsevier."

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SiCN charge trapping film. In addition, the J_g-V_g curve measured with a long delay time of 60 s at every step is shown in Fig. 2.8(a). At the second scan, the displacement current component almost disappeared with the long delay time and the leakage current component showed up at high voltages. During the long delay time at every step, holes would be injected into the SiCN film and would fill many trap centers. After the lapse of the delay time, the density of empty trap centers ought to be decreased. Moreover, a positive charge would be generated in the SiCN film by the trapped holes. These two phenomena certainly decrease the probability of hole tunneling from the silicon substrate to empty trap centers. Therefore, the displacement current component attributed to hole trapping was substantially decreased and was hardly detected.

From the CV curve shown in Fig. 2.5(a), the value of $V_{fb,0}$ was obtained to be -3.4 V for the SiCN capacitor. This result indicates that a fixed positive charge was present in the stacked films even after baking the capacitor for a long period in time. Ma and co-workers reported that the flat-band voltage is shifted from its ideal value by fixed positive charges primarily at the two oxide-nitride interfaces in the oxide-silicon nitride-oxide stacked films [31]. Therefore, assuming that the amount of the fixed positive charge distributed at the tunnel oxide-charge trapping film interface is the same as that distributed at the blocking oxide-charge trapping film interface, the charge centroid of fixed positive charges $\bar{x}_{fix}$ is located at the middle of the charge trapping film. Then, the electric field in the blocking oxide film of the SiCN capacitor induced by the fixed positive charges, ΔE_{fix}, is estimated to be 0.30 MV/cm using the following equations:

$$\Delta E_{fix} = -\frac{t_{tn} + \dfrac{\varepsilon_{box}}{\varepsilon_{ctl}}\left(t_{ctl} - \bar{x}_{fix}\right)}{t_{eq}} \frac{\left(V_{fb,0} - \phi_{ms}\right)}{t_{box} + \dfrac{\varepsilon_{box}}{\varepsilon_{ctl}}\bar{x}_{fix}} \tag{2.11}$$

and

$$\bar{x}_{fix} = \frac{t_{ctl}}{2}.$$

(2.12)

Here, t_{tn} and t_{ctl} are the thicknesses of the tunnel oxide film and the charge trapping film respectively and ϕ_{ms} is the metal-semiconductor work function deference. In addition, during the J_g-V_g measurement, holes were captured by trap centers and an additional positive charge was built up in the SiCN film. The energy band diagrams of the aluminum-blocking oxide-SiCN-tunnel oxide-silicon structure at the flat-band condition and a negative gate voltage of -18 V are shown in Figs. 2.9(a) and 2.9(b). In Fig. 2.9(b), the fixed positive charge and trapped holes are drawn as sheet charges. It is revealed that electrons can be injected through the blocking oxide film at negative gate voltages. Taking into account the presence of the fixed positive charge and trapped holes, the Fowler-Nordheim (FN) tunneling current J_{FN} consisting of electrons injected from the gate electrode is given by the following equations:

$$J_{FN} = \left(\frac{q^3 m}{8\pi h \Phi_b m_{ox}} \right) E_{box}^{\ 2} \exp\left(-\frac{4\sqrt{2m_{ox}}\Phi_b^{\ 3/2}}{3q\hbar E_{box}} \right)$$

(2.13)

and

$$E_{box} = -\frac{V_g - \phi_{ms}}{t_{eq}} + \Delta E_{fix} + \Delta E_{hole},$$

(2.14)

where E_{box} is the electric field in the blocking oxide film, Φ_b is the energy barrier height for electrons, m and m_{ox} are the electron mass in free space and in SiO_2 respectively, q is the elementary charge, h is the Planck constant, $\hbar$ is the reduced Planck constant, ΔE_{hole} is the electric field in the blocking oxide film induced by the trapped holes and t_{eq} is the oxide-equivalent thickness of the stacked films. The broken line in Fig. 2.8(a) shows J_{FN}

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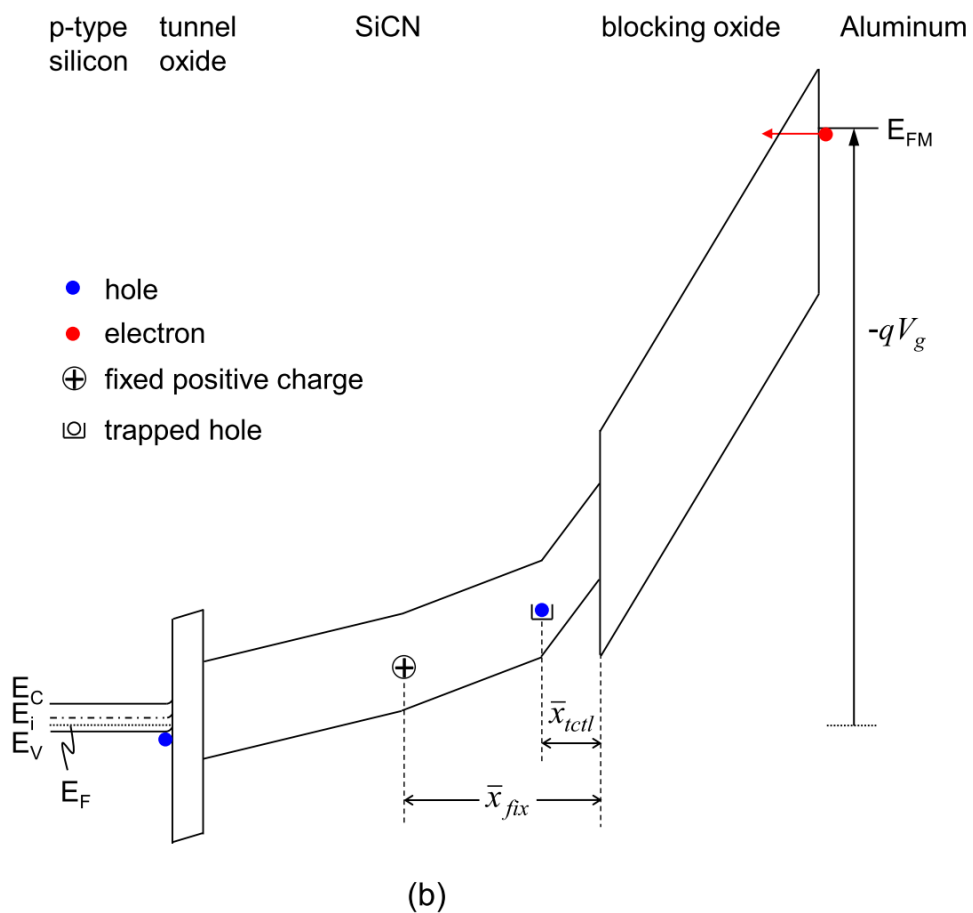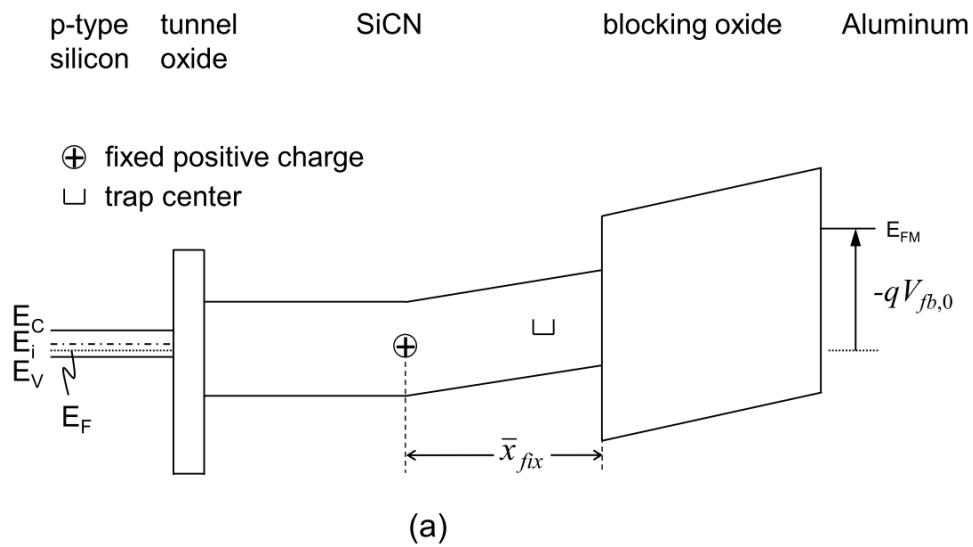
Fig. 2.9 (a) Energy band diagram of the aluminum-blocking oxide-SiCN-tunnel oxide-silicon structure at flat-band condition. (b) Energy band diagram of the aluminum-blocking oxide-SiCN-tunnel oxide-silicon structure at a negative gate voltage of -18 V.

as a function of V_g, which was calculated using Eqs. (2.13) and (2.14). The calculated FN current was in good agreement with the gate current density measured at high gate voltages, which was obtained with ΔE_{hole} of 3.24 MV/cm and the following parameters. The Φ_b value was estimated to be 3.4 eV using the aluminum work function of 4.28 eV [32] and the energy difference between the SiO$_2$ conduction band and the vacuum level [33,34]. The electron effective mass $m_{ox} = 0.42\ m$ was used [35]. $Q_{leak}(t_0,t_1)$ was estimated using the values of J_{FN} calculated for the gate voltages during hole injection shown in Fig. 2.7(a).

From the CV curve in Fig. 2.5(b), the value of $V_{fb,0}$ was determined to be -4.4 V for the silicon nitride capacitor. The ΔE_{fix} value is estimated to be 0.42 MV/cm using Eqs. (2.11) and (2.12). In Fig. 2.8(b), the broken line shows the calculated result of J_{FN} consisting of electrons injected through the blocking oxide film into the silicon nitride film. The good agreement between the measured result and the calculation was obtained with ΔE_{hole} of 2.20 MV/cm. $Q_{leak}(t_0,t_1)$ in the silicon nitride capacitors was also estimated using the values of J_{FN} calculated for the gate voltages during hole injection shown in Fig. 2.7(b).

The ΔE_{hole} value of 3.24 MV/cm used for the SiCN capacitor can be generated by trapped holes of 1.3×10^{13} cm^{-2} assuming $\overline{x}_{tctl}$ of 5 nm. The ΔE_{hole} value for the silicon nitride capacitor can also be generated by trapped holes of 1.2×10^{13} cm^{-2} located at $\overline{x}_{tctl}$ of 8 nm. As will be shown later in the experimental result of Fig. 2.12, $\overline{x}_{tctl}$ was actually located near the blocking oxide-charge trapping film interface after a large number of holes were injected into the charge trapping film. According to the literature from Ishida

et al., holes of 1.7×10^{13} cm^{-2} in density can be trapped in the oxide-nitride-oxide structure with a 30-nm thick silicon nitride film [36]. Therefore, the densities of trapped holes calculated for the SiCN and silicon nitride capacitors are acceptable. Then, the ΔE_{hole} values used in the calculations of the present study are acceptable also.

2.3.3 Charge centroid of trapped holes after hole injection

Figure 2.10(a) shows the relationship between $V_{fb,h1}$ and the number of injected holes per unit area F_{inj} in the SiCN capacitors subjected to the constant-current hole injection. F_{inj} is calculated by

$$F_{inj} = \frac{Q_{inj}(t_0,t_1)}{q}. \qquad (2.15)$$

Figure 2.10(b) shows $V_{fb,h1}$ as a function of F_{inj} in the silicon nitride capacitors subjected to the constant-current hole injection. The experimental results in the case that the $Q_{leak}(t_0,t_1)$ values were smaller than 1 % of $Q_{inj}(t_0,t_1)$ are plotted in Figs. 2.10(a) and 2.10(b). It is considered that the criterion of 1 % of $Q_{inj}(t_0,t_1)$ is small enough to use the
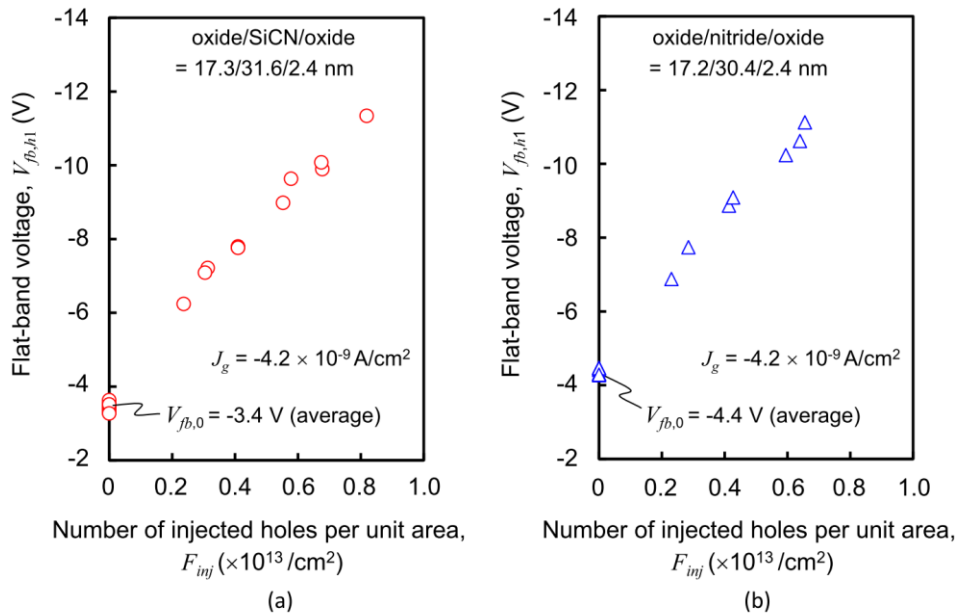
Fig. 2.10 (a) Flat-band voltage $V_{fb,h1}$ as a function of the number of injected holes per unit area F_{inj} in the SiCN capacitors subjected to the constant-current hole injection. (b) $V_{fb,h1}$ as a function of F_{inj} in the silicon nitride capacitors subjected to the constant-current hole injection.

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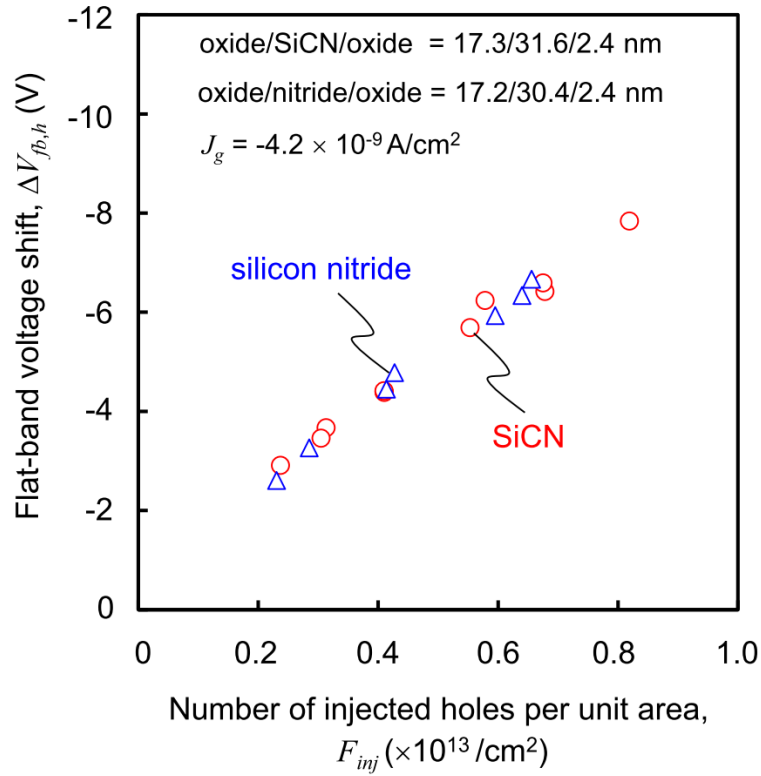
Fig. 2.11 $\Delta V_{fb,h}$ versus F_{inj} in the SiCN and silicon nitride capacitors subjected to the constant-current hole injection. This Figure is "Reproduced with permission from ECS Transactions, 75(32), 51 (2017). Copyright 2017, The Electrochemical Society."

relationship given by Eq. (2.9). Thus, it is claimed that most of holes injected to the SiCN and silicon nitride charge trapping films were captured by trap centers and contributed to the variation of $V_{fb,h1}$. Figure 2.11 shows $\Delta V_{fb,h}$ versus F_{inj} in the SiCN and silicon nitride capacitors subjected to the constant-current hole injection. $\Delta V_{fb,h}$ monotonously increased with increasing F_{inj} in the both capacitors. It should be noted that the $\Delta V_{fb,h}$ values in the SiCN capacitors almost coincided with those in the silicon nitride capacitors.

The charge centroid $\bar{x}_{tctl}$ of trapped holes was calculated by using Eq. (2.10) and the $\Delta V_{fb,h}$ values shown in Fig. 2.11, and is plotted as a function of F_{inj} in Fig. 2.12. It can be seen that $\bar{x}_{tctl}$ in the SiCN capacitors was located at 11 nm at 0.24×10^{13} cm^{-2} in F_{inj},

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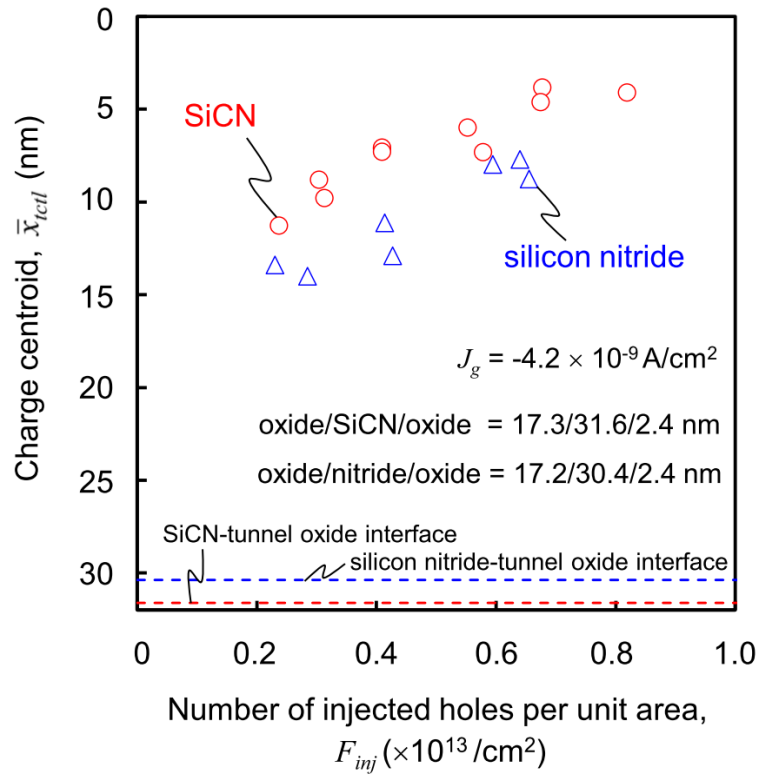
Fig. 2.12 Charge centroid $\bar{x}_{tctl}$ of trapped holes as a function of F_{inj} in the SiCN and silicon nitride capacitors subjected to the constant-current hole injection.

and then gradually shifted toward the blocking oxide-SiCN interface with the increase in F_{inj}. On the other hand, $\bar{x}_{tctl}$ in the silicon nitride capacitors was initially located at 13 nm and moved toward the blocking oxide-silicon nitride interface with the increase in F_{inj}. It should be noted that $\bar{x}_{tctl}$ in the SiCN capacitors was closer to the interface as compared to that in the silicon nitride capacitors. In the following section 2.3.4, the distribution of holes trapped in the charge trapping films will be discussed.

2.3.4 Comparisons of movement of charge centroid of holes trapped in charge trapping films

Figures 2.13(a), 2.13(b) and 2.13(c) show the schematic representation showing the spatial distributions of holes captured by empty trap centers in the SiCN charge trapping film for different values of F_{inj}. As described in section 2.2.3, the sample capacitors were baked and trap centers were initially empty, as shown in Fig. 2.13(a). From the experimental result in Fig. 2.12, $\bar{x}_{tctl}$ in the SiCN film was located at 11 nm from the blocking oxide-SiCN interface at F_{inj} of 0.24×10^{13} cm^{-2}. Since, there is little knowledge of the spatial distribution of trapped holes except for $\bar{x}_{tctl}$, the hole distribution is assumed to have a Gaussian-like distribution around $\bar{x}_{tctl}$ to discuss the hole trapping and transport phenomena in the SiCN film, as shown in Fig. 2.13(b). In Fig. 2.12, $\bar{x}_{tctl}$ in the SiCN film was shifted to the location of 5 nm at F_{inj} of 0.68×10^{13} cm^{-2}. $\bar{x}_{tctl}$ of 5 nm would require a tight hole distribution in the vicinity of the blocking oxide-SiCN interface shown in Fig. 2.13(c). The applied gate voltage reached -15.1 V during the hole injection, and the average electric field $\bar{E}$ in the SiCN film at that time was estimated to be 3.8 MV/cm (see Appendix). Therefore, holes injected from the silicon substrate in the SiCN film would be transported toward the blocking oxide-SiCN interface. In addition, from the comparison between the hole distributions in Figs. 2.13(b) and 2.13(c), it is considered that holes which were captured once by trap centers also moved toward the interface during applying negative gate bias.

On the other hand, the spatial distributions of holes captured by empty trap centers in the silicon nitride charge trapping film after hole injection at different values of F_{inj} were represented in Figs. 2.14(a), 2.14(b) and 2.14(c). After the baking, the trap centers in the
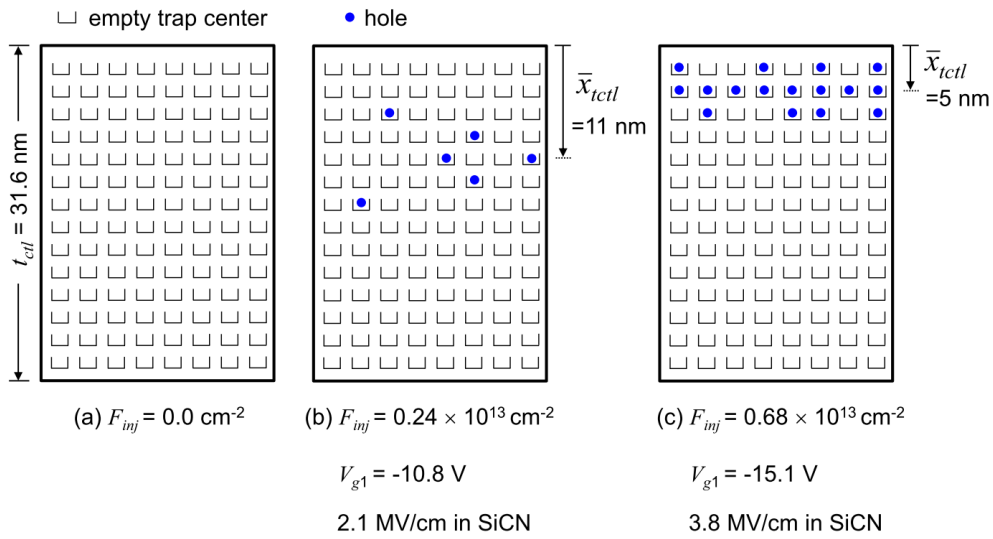
Fig. 2.13 Schematic representations showing the spatial distributions of holes captured by empty trap centers in the SiCN charge trapping film after hole injection at different values of F_{inj}: (a) 0.0 cm^{-2}, (b) 0.24 × 10^{13} cm^{-2}, and (c) 0.68 × 10^{13} cm^{-2}.
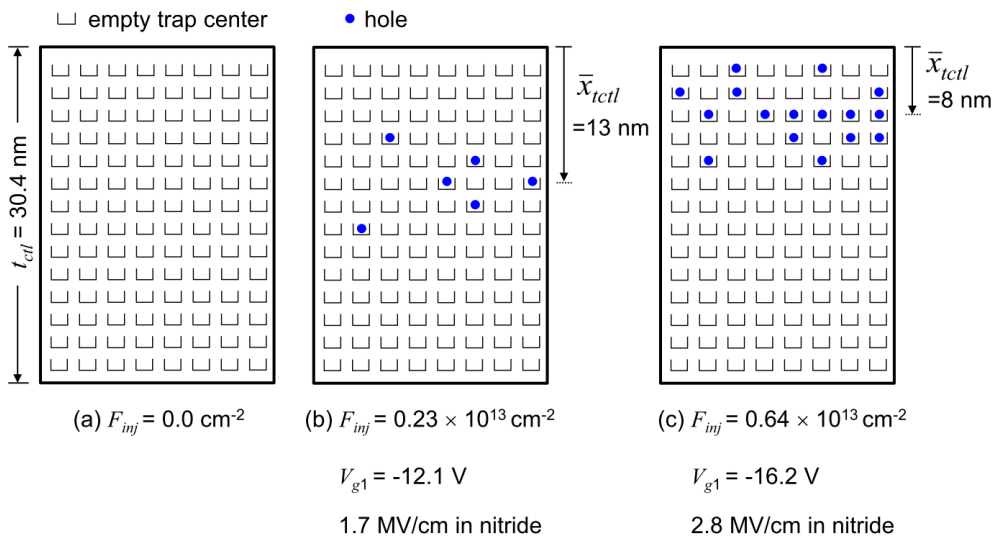
Fig. 2.14 Schematic diagrams illustrating the spatial distributions of holes captured by empty trap centers in the silicon nitride charge trapping film after hole injection at different values of F_{inj}: (a) 0.0 cm^{-2}, (b) 0.23 × 10^{13} cm^{-2}, and (c) 0.64 × 10^{13} cm^{-2}.

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silicon nitride film were empty as shown in Fig. 2.14(a). In Fig. 2.12, $\bar{x}_{tctl}$ in the silicon

nitride film at F_{inj} of 0.23×10^{13} cm^{-2} was located at 13 nm. The trapped holes were

assumed to be distributed around $\bar{x}_{tctl}$, as shown in Fig. 2.14(b). At F_{inj} of 0.64×10^{13}

cm^{-2}, $\bar{x}_{tctl}$ was changed to the location of 8 nm. Fig. 2.14(c) represents the hole

distribution around $\bar{x}_{tctl}$ of 5 nm in the silicon nitride film. During the hole injection, the

gate voltage was obtained to be -16.2 V. $\bar{E}$ in the silicon nitride film at the gate voltage

was calculated to be 2.8 MV/cm (see Appendix). Consequently, holes injected from the

silicon substrate in the silicon nitride film would be transported toward the blocking

oxide-silicon nitride interface. In Figs. 2.14(b) and 2.14(c), holes which were trapped

previously by trap centers also shifted toward the blocking oxide-silicon nitride interface

during applying negative gate bias.

As shown in Figs. 2.13(b), 2.13(c), 2.14(b) and 2.14(c), the hole distribution in the

SiCN film was closer to the blocking oxide-SiCN interface as compared to that in the

silicon nitride film. As was mentioned in section 2.2.1, the dielectric constant of the SiCN

film is 4.8, which is lower than that of the silicon nitride film. Therefore, the electric field

in the SiCN film would be higher than that of the silicon nitride film when a fixed voltage

is applied to the gate electrode. At the stages shown in Figs. 2.13(b) and 2.14(b), the gate

voltages of -10.8 and -12.1 V were applied to the SiCN and silicon nitride capacitors,

respectively. The values of $\bar{E}$ in the SiCN and silicon nitride films were estimated to be

2.1 and 1.7 MV/cm, respectively, using the equations in Appendix. Although the applied

gate voltage of the SiCN capacitor was smaller than that of the silicon nitride capacitor,

$\bar{E}$ in the SiCN film was obtained to be larger due to the effect of the lower dielectric

constant of the SiCN film. The values of $\overline{E}$ under the gate voltages of -15.1 and -16.2 V were calculated to be 3.8 and 2.8 MV/cm in the SiCN and silicon nitride films, respectively, with regard to Figs. 2.13(c) and 2.14(c). In addition, it can be considered that the hole transport in the SiCN and silicon nitride charge trapping films was dominated by the Poole-Frenkel (PF) conduction mechanism. The probability of the PF emission of holes from trap states, P, is given by

$$P \propto exp\left[\frac{-q(\phi_t - \sqrt{qE/\pi\varepsilon_0\varepsilon_d})}{k_B T}\right],$$
(2.16)

where E is the electric field in dielectric films, ϕ_t is the energy depth of the trap centers, ε_d is the dynamic relative dielectric constant, k_B is the Boltzmann constant, and T is the temperature. In the previous report, the dynamic relative dielectric constant of the SiCN film was found to be 4.4 [37]. This value was lower as compared with 5.5±1 of the silicon nitride film [38]. Moreover, the energy depth of trap centers for holes related to the PF conduction in the SiCN film was obtained to be 0.8 eV [37], which was shallower as compared with the trap depth of 1.0-1.3 eV in silicon nitride films [38,39]. Therefore, it is suggested that holes injected into the SiCN film were easily transported toward the blocking oxide-SiCN interface by the PF conduction. The high electric field, the low dynamic dielectric constant and the presence of the shallow trap centers would be responsible for $\overline{x}_{tctl}$ close to the blocking oxide-SiCN interface.

As shown in Fig. 2.11, the flat-band voltage shift $\Delta V_{fb,h}$ in the SiCN capacitors coincided with that in the silicon nitride capacitors. According to Eqs. (2.1) and (2.10), $\Delta V_{fb,h}$ is represented by

$$\Delta V_{fb,h} = -\left(\frac{t_{box}}{\varepsilon_0 \varepsilon_{box}} + \frac{\overline{x}_{tctl}}{\varepsilon_0 \varepsilon_{ctl}}\right) q F_{inj} \,. \qquad (2.17)$$

This equation indicates that $\Delta V_{fb,h}$ is functions of $\overline{x}_{tctl}$ and ε_{ctl}. As shown in Fig. 2.12, $\overline{x}_{tctl}$ of holes trapped in the SiCN capacitors was smaller than that in the silicon nitride capacitors. On the other hand, as described in section 2.2.1, the ε_{ctl} value of the SiCN film was lower than that of the silicon nitride film. As a result, $\Delta V_{fb,h}$ in the SiCN capacitors was almost the same as that in the silicon nitride capacitors. To obtain a larger $\Delta V_{fb,h}$ in the SiCN capacitors, it would be effective to decrease the ε_{ctl} value of the SiCN film by increasing the chemical composition ratio of carbon in the film.

As mentioned in section 2.1, it was reported that the erasing speed in the SiCN capacitors was obviously higher than that in the silicon nitride capacitors [17,18]. However, as described above, almost the same $\Delta V_{fb,h}$-F_{inj} characteristics was obtained in the both capacitors. The higher speed of hole injection in the SiCN capacitors compared to that in the silicon nitride capacitors might be a possible explanation for the high erasing speed in the SiCN capacitor. Further study on the hole injection mechanism would be required to understand the erasing operation in the SiCN-based memories.

Additionally, in the present study, although the charge centroid of trapped holes was evaluated by using the constant-current carrier injection method, the hole distribution in the charge trapping films cannot be discussed quantitatively. Further investigation of the hole distribution would also be needed for fully understanding of the detailed mechanisms of the erasing operation.

In this chapter, the constant-current carrier injection method was proposed to obtain the charge centroid of carriers trapped in the charge trapping films and to count the number of carriers injected to the films. It was revealed that the constant-current carrier

injection method is useful for obtaining the accurate charge centroid of carriers trapped in the charge trapping films. The charge centroid of carrier trapped in the charge trapping films is an important information for understanding the charge trapping mechanism in programming and erasing operations of NVMs.

2.4 Conclusions

In this chapter, the constant-current carrier injection method was proposed to obtain the charge centroid of trapped carriers in stacked dielectric films and to count the number of carriers injected to the stacked films. To get a better understanding of the mechanisms of erasing operation, the proposed method was used and the charge centroid $\bar{x}_{tctl}$ of holes trapped in the SiCN and silicon nitride charge trapping films with only empty trap centers was extracted. $\bar{x}_{tctl}$ was initially located near the middle of the SiCN and silicon nitride films, and moved toward the blocking oxide-SiCN interface or the blocking oxide-silicon nitride interface with increasing the number of injected holes per unit area F_{inj}.

It was also found that $\bar{x}_{tctl}$ in the SiCN film was closer to the blocking oxide-SiCN interface as compared to that in the silicon nitride film. The location of $\bar{x}_{tctl}$ in the SiCN film is explained by the model that holes were easily transported toward the blocking oxide-SiCN interface because of the high electric field, the low dynamic dielectric constant and the presence of the shallow trap centers involved in the PF conduction in the SiCN film.

The flat-band voltage shift in the SiCN capacitors almost coincided with that in the silicon nitride capacitors. This result is interpreted as results of the smaller value of $\bar{x}_{tctl}$ and the lower static dielectric constant of the SiCN film than those of the silicon nitride film.

The hole trapping characteristics in the SiCN and silicon nitride films with empty trap centers was quantitatively evaluated using the constant-current carrier injection method.

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Appendix

The average electric field $\overline{E}$ in the charge trapping films is given by

$$\overline{E} = E_1 + E_2 + E_3, \tag{A.1}$$

$$E_1 = \frac{V_{fb,0} - \phi_{ms}}{\dfrac{\varepsilon_{ctl}}{\varepsilon_{box}} \cdot t_{box} + \dfrac{1}{2} t_{ctl}}, \tag{A.2}$$

$$E_2 = \frac{\Delta V_{fb,h}}{\dfrac{\varepsilon_{ctl}}{\varepsilon_{box}} \cdot t_{box} + \overline{x}_{tctl}} \quad \text{and} \tag{A.3}$$

$$E_3 = \frac{V_{g1} - V_{fb,h1}}{t_{ctl} + (t_{box} + t_{tn}) \cdot \dfrac{\varepsilon_{ctl}}{\varepsilon_{box}}}. \tag{A.4}$$

In Eq. (A.2), the electric field E_1 in the charge trapping films is generated by the fixed positive charges. It is assumed that the amount of the fixed positive charge distributed at the tunnel oxide-charge trapping film interface is the same as that distributed at the blocking oxide-charge trapping film interface. Then, the charge centroid of fixed positive charges $\overline{x}_{fix}$ is assumed to be located at the middle of the charge trapping film, $\overline{x}_{fix} = \frac{1}{2} t_{ctl}$. In Eq. (A.3), the electric field E_2 is generated by holes trapped in the charge trapping films. In Eq. (A.4), the electric field E_3 is generated due to additional gate voltage applied to the capacitors. Figures A.1(a), A.1(b) and A.1(c) show the energy band diagrams of the aluminum-blocking oxide-SiCN-tunnel oxide-silicon structure at the flat-band condition and negative gate voltage. The electric fields E_1, E_2 and E_3 generated by the fixed positive charges, the trapped holes and the additional gate voltage are shown in Figs. A.1(a), A.1(b) and A.1(c).
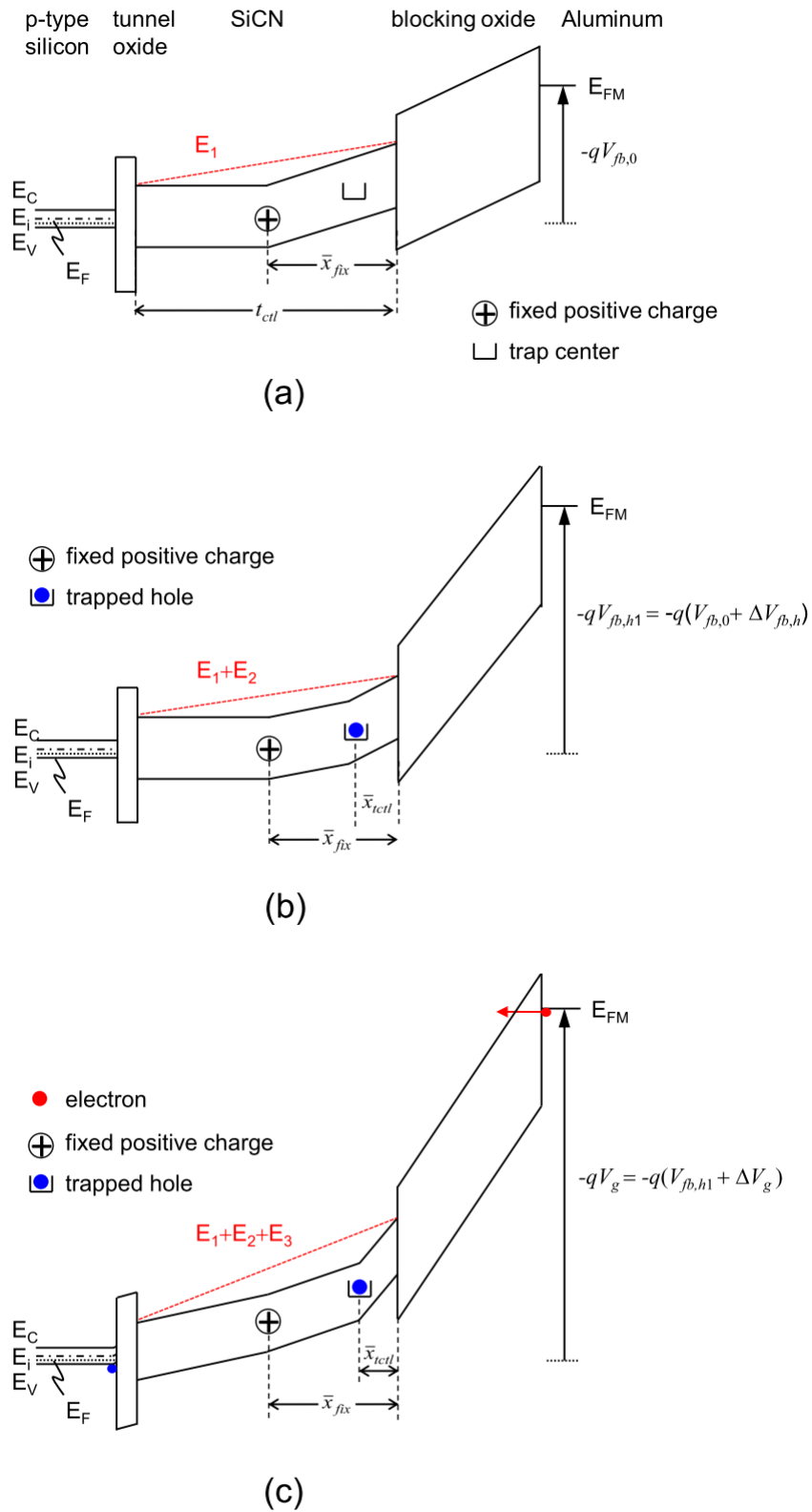
Fig. A.1 (a) Energy band diagram of the aluminum-blocking oxide-SiCN-tunnel oxide-silicon structure at flat-band condition. (b) and (c) Energy band diagrams of the aluminum-blocking oxide-SiCN-tunnel oxide-silicon structure at negative gate voltages.

Chapter **3**

Hole trapping characteristics of SiCN films with both trap centers filled by electrons and empty trap centers

Chapter 3　Hole trapping characteristics of SiCN films with both trap centers filled by electrons and empty trap centers

3.1　Introduction

As was mentioned in section 1.2 in chapter 1, memory cell size in the MONOS-type devices is becoming smaller to meet the requirements of high capacity and low cost. Consequently, the amount of charges stored in memory transistors is decreasing. Thus, it is important to understand the charge trapping mechanisms to ensure sufficient charge storage in small size transistors of embedded NVMs.

In the last few decades, several studies have been made on the erasing characteristics of MONOS devices after the programming operation [1-11]. In the previous chapters, it was mentioned that there are three charge states of trap centers in the charge trapping films, namely empty trap centers, trap centers filled by electrons and trap centers filled by holes. Both the empty trap centers and the trap centers filled by electrons would exist in the silicon nitride films after the programming operation.

In chapter 2, to get a better understanding of the carrier trapping mechanisms during erasing operation, the charge centroid of holes trapped in the SiCN and silicon nitride charge trapping films with only empty trap centers was extracted by using the constant-current carrier injection method. In this chapter, the hole trapping characteristics in the SiCN and silicon nitride films with both trap centers filled by electrons and empty trap centers were studied. In addition, the constant-current carrier injection method presented in chapter 2 was used to investigate the electron elimination phenomenon in the erasing operation of the SiCN and silicon nitride memory capacitors.

In this chapter, the fabrication conditions of memory capacitors and the procedures

for measuring the hole trapping characteristics in the two conditions of the charge trapping films will be first introduced in section 3.2. Next, the flat-band voltage shift in the SiCN and silicon nitride memory capacitors in the two conditions after the constant-current carrier injection will be discussed by analyzing the CV characteristics in section 3.3.1. Then, to count the number of holes injected to the charge trapping films, the constant-current carrier injection method proposed in section 2.3.1 in chapter 2 will be explained in brief. In section 3.3.3, the hole trapping and the electron elimination phenomenon in the erasing operation of the SiCN and silicon nitride memory capacitors will be discussed. Finally, conclusions of this chapter will be provided.

3.2 Experimental details

3.2.1 Sample fabrication

The same conditions of the sample fabrication as described in section 2.2.1 in chapter 2 are repeated in this section. Memory capacitors with blocking oxide-SiCN-tunnel oxide and blocking oxide-silicon nitride-tunnel oxide stacked films were fabricated on p-type (100) silicon substrates. Figure 3.1 shows the schematic representation of the memory capacitor used in this study. A 2.4-nm-thick tunnel oxide film was formed by rapid thermal oxidation at 1050 °C of the silicon substrates in both types of the stacked dielectric films. A 31.6-nm-thick SiCN film was grown at 400 °C using $Si(CH_3)_4$ and NH_3 gases by PECVD. A 30.4-nm-thick silicon nitride film was formed by LPCVD using of Si_2Cl_6 and NH_3 gases at 600 °C. A blocking oxide film of 17.2-17.3 nm in thickness was grown at 400 °C by PECVD. Finally, an aluminum film was deposited by thermal evaporation through a metal mask (shadow mask evaporation) to form the gate electrode.
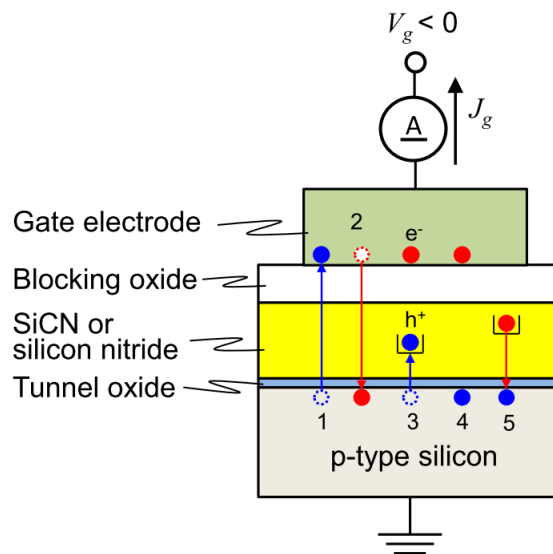
Fig. 3.1 Schematic representation of the SiCN or silicon nitride memory capacitor used in this study. The number 5 indicates the elimination of electrons from trap centers.

3.2.2 Procedures for measuring hole trapping characteristics of two conditions

Two sets of experiments were performed on the fabricated capacitors. Figures 3.2(a) and 3.2(b) show the experimental procedures. In the first experiment, after the sample fabrication, all the memory capacitors were baked in air at 235 °C for a long period of time to emit electrons and holes trapped in the blocking oxide-SiCN-tunnel oxide and the blocking oxide-silicon nitride-tunnel oxide stacked films, as shown in Fig. 3.2(a). The high-frequency capacitance-voltage (CV) measurements were conducted and the flat-band voltage $V_{fb,0}$ of the baked capacitors was determined. At the next step, the gate electrodes were negatively biased to inject holes from the silicon substrates into the charge trapping films at a constant gate current density of -4.2 × 10^{-9} A/cm^2. After holes injection following the baking, the CV characteristics were again measured to determine the flat-band voltage $V_{fb,h1}$. The hole injection following the baking is termed HI-BK.

In the second experiment, after the sample fabrication, all the memory capacitors were baked at 235 °C for a long period of time to empty all trap centers existing in the charge trapping films. After the memory capacitors were baked, the CV characteristics were measured and the flat-band voltage $V_{fb,0}$ of the baked capacitors was determined, as shown in Fig. 3.2(b). The gate electrodes were positively biased with visible light illumination to inject electrons from the silicon substrates into the charge trapping films at a constant gate current density of +4.2 × 10^{-9} A/cm^2. After the electron injection, the CV characteristics were measured to determine the flat-band voltage $V_{fb,e1}$. Next, the gate electrodes were biased negatively to inject holes into the charge trapping films at a constant gate current density of -4.2 × 10^{-9} A/cm^2. After the negative voltage was applied, the CV characteristics were measured to determine the flat-band voltage $V_{fb,h1}$. The hole injection following the electron injection is termed HI-EI. The CV characteristics were

measured at 100 kHz with an Agilent E4980 LCR meter.

● Baking the sample capacitors at 235 °C
    Trapped carriers in the stacked films were emitted.

○ CV measurement (100 kHz)
    The flat-band voltage was determined: $V_{fb,0}$

● Constant-current hole injection at -4.2×10^{-9} A/cm^2
    The gate was negatively biased to inject holes to
    the charge trapping film.

○ CV measurement (100 kHz)
    After hole injection, $V_{fb,h1}$ was measured to determine $\Delta V_{fb,h}$.

● The injected charge per unit area Q_{inj} was calculated.

(a)

● Baking the sample capacitors at 235 °C
    Trapped carriers in the stacked films were emitted.

○ CV measurement (100 kHz)
    The flat-band voltage was determined: $V_{fb,0}$

● Constant-current electron injection at $+4.2 \times 10^{-9}$ A/cm^2
    The gate was positively biased to inject electrons to the
    charge trapping film.

○ CV measurement (100 kHz)
    After electron injection, $V_{fb,e1}$ was measured to determine $\Delta V_{fb,e}$.

● Biasing the gate negatively
    The gate voltage was changed to keep a gate current
    -4.2×10^{-9} A/cm^2.

○ CV measurement (100 kHz)
    After a negative gate voltage was applied, $V_{fb,h1}$ was measured
    to determine $\Delta V_{fb,h}$.

● The injected charge per unit area Q_{inj} was calculated.

(b)

Fig. 3.2 Experimental procedures to measure $\Delta V_{fb,h}$ as a function of F_{inj} in the SiCN or silicon nitride memory capacitor subjected to (a) HI-BK and (b) HI-EI. Figures 3.2(a) and 3.2(b) are "Reproduced with permission from ECS Transactions, 75(32), 73 (2017). Copyright 2017, The Electrochemical Society."

3.3 Results and discussion

3.3.1 Capacitance-voltage characteristics of memory capacitors

Figure 3.3(a) shows the CV characteristics of the SiCN memory capacitor after the baking at 235 °C and after hole injection following the baking (HI-BK). To empty all trap centers existing in the SiCN film, the 235 °C baking of the capacitor and the CV measurement were conducted alternately. Then, it was confirmed that the flat-band voltage converged to a value of -3.4 V, which is termed as $V_{fb,0}$. After HI-BK, holes were injected from the silicon substrate to the SiCN charge trapping film. The flat-band voltage was shifted toward the negative voltage direction from $V_{fb,0}$ to $V_{fb,h1}$ due to holes captured by empty trap centers in the SiCN charge trapping film. The flat-band voltage shift $\Delta V_{fb,h}$ was derived from the difference between $V_{fb,0}$ and $V_{fb,h1}$.

Figure 3.3(b) shows the CV characteristics of the SiCN memory capacitor after the baking, after the subsequent electron injection and after the constant-current hole injection following the electron injection (HI-EI). The flat-band voltage was shifted toward the positive voltage direction from $V_{fb,0}$ to $V_{fb,e1}$ after the electron injection. This shift is attributed to electron capture by trap centers in the SiCN film. The flat-band voltage shift $\Delta V_{fb,e}$ was calculated from $V_{fb,0}$ and $V_{fb,e1}$, and ranged from 3.0 to 3.5 V. After HI-EI, the flat-band voltage was shifted toward the negative voltage direction. $\Delta V_{fb,h}$ was obtained from the difference between $V_{fb,e1}$ and $V_{fb,h1}$.
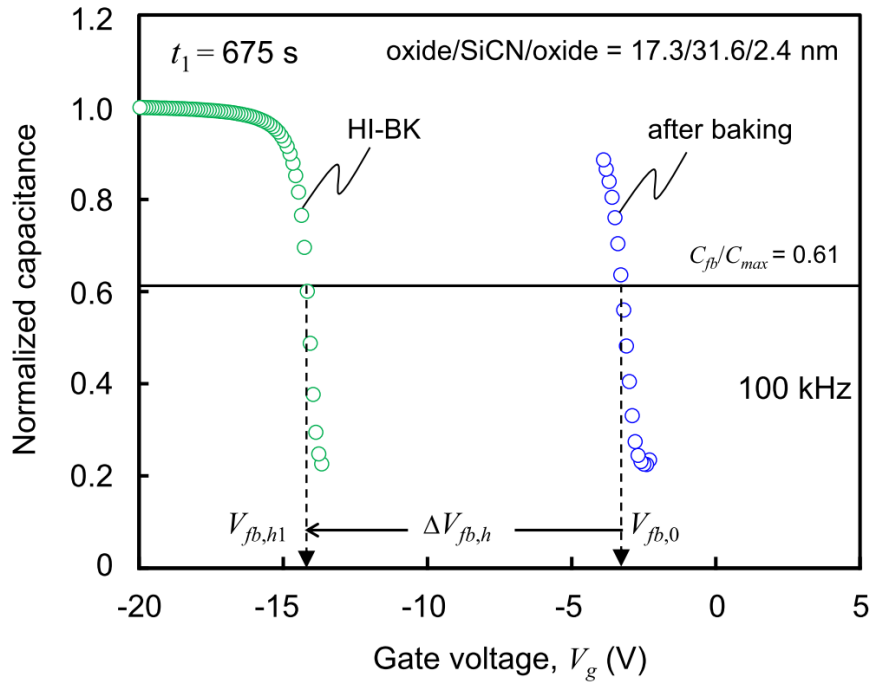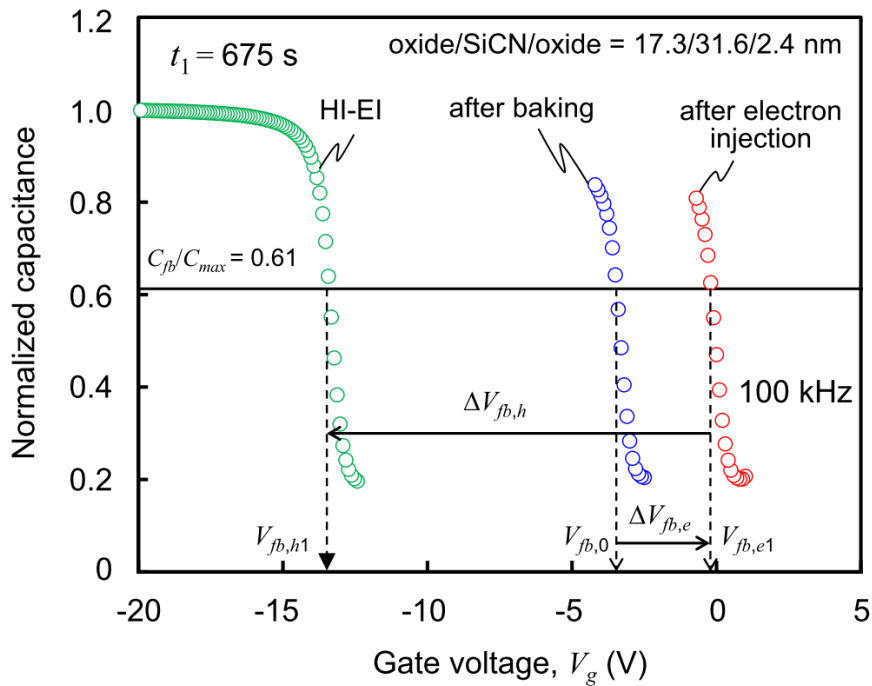
Fig. 3.3 (a) CV characteristics of the SiCN memory capacitor subjected to the constant-current hole injection following the baking (HI-BK). (b) CV characteristics of the SiCN memory capacitor subjected to the constant-current hole injection following the electron injection (HI-EI).

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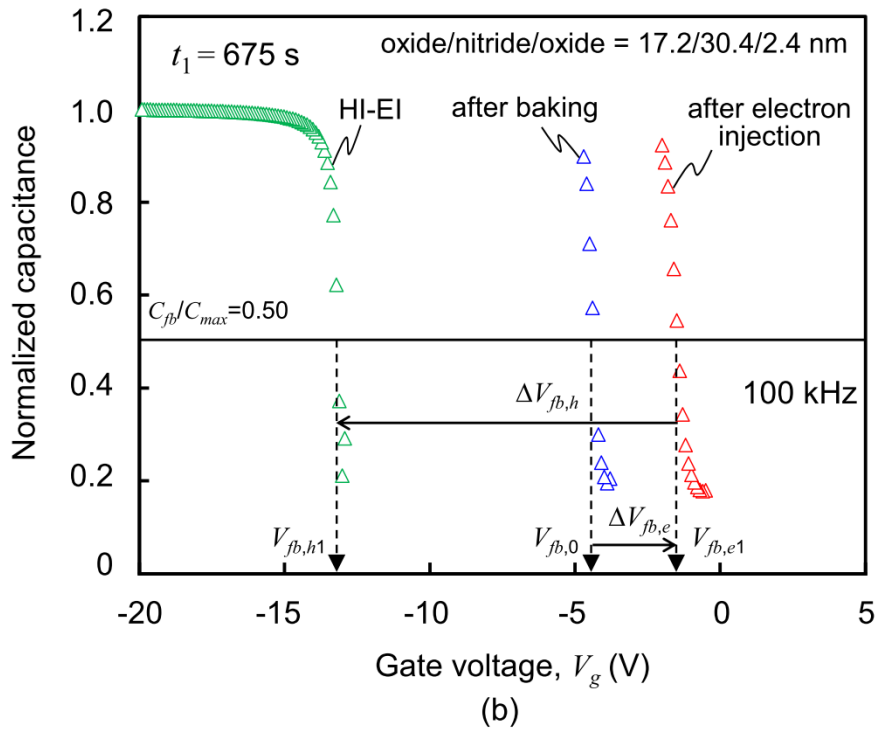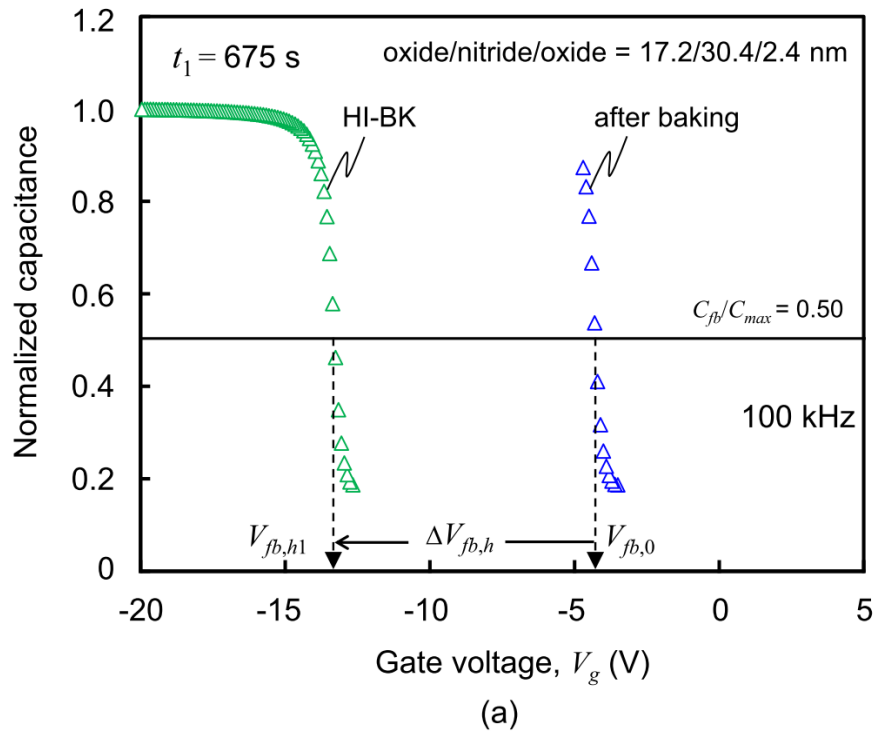
Fig. 3.4 (a) CV characteristics of the silicon nitride memory capacitor subjected to HI-BK. (b) CV characteristics of the silicon nitride memory capacitor subjected to HI-EI.

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Figure 3.4(a) shows the CV characteristics of the silicon nitride capacitor subjected to HI-BK. As mentioned in section 3.2.2, after the sample fabrication, all the memory capacitors were baked at 235 °C to empty all trap centers existing in the charge trapping film. The 235 °C baking of the capacitor and the CV measurement were carried out alternately and $V_{fb,0}$ of -4.3 V in the silicon nitride capacitor was determined. After HI-BK, $\Delta V_{fb,h}$ induced by holes trapped in the silicon nitride charge trapping film was obtained from the difference between $V_{fb,0}$ and $V_{fb,h1}$.

Figure 3.4(b) shows the CV characteristics of the silicon nitride capacitor after the baking, after the subsequent electron injection, and after HI-EI. After electron injection, $\Delta V_{fb,e}$ was calculated from $V_{fb,0}$ and $V_{fb,e1}$, and ranged from 2.7 to 3.4 V. After HI-EI, the flat-band voltage was shifted toward the negative voltage direction. In Fig. 3.4(b), $\Delta V_{fb,h}$ was determined from the difference between $V_{fb,e1}$ and $V_{fb,h1}$.

3.3.2 Constant-current carrier injection method to count number of holes injected to charge trapping films

Figure 3.5(a) shows the gate voltage shift of the SiCN capacitor during the constant-current hole injection following the baking. The gate voltage shift of the silicon nitride capacitor during HI-BK is also shown in Fig. 3.5(b). Here, $Q_{meas}(t)$ is defined with the gate current density J_g and hole injection time t, as described in Eq. (2.3) in section 2.3.1 in chapter 2. In Figs. 3.5(a) and 3.5(b), the gate voltage V_g increased with increasing $Q_{meas}(t)$. In both the capacitors, the silicon surface was under the inversion or depletion condition while V_g ranged from 0 to $V_{fb,0}$. When V_g was larger than $V_{fb,0}$ in Figs. 3.5(a) and 3.5(b), the silicon surface was in the accumulation condition and holes were injected from the silicon substrates into the charge trapping films through the thin tunnel oxide film via the quantum mechanical tunneling. In Figs. 3.5(a) and 3.5(b), the definition of $Q_{meas}'(t_0, t_1)$ was described in Eq. (2.4) in section 2.3.1 in chapter 2. Then, using the Eqs. (2.5)-(2.8) and (2.15) described in sections 2.3.1 and 2.3.3 in chapter 2, the number of injected holes per unit area F_{inj} for HI-BK is calculated.

On the other hand, in the case of HI-EI, some of trap centers filled by electrons would emit electrons to the silicon substrate under the negative gate bias. The electron flow ought to contribute to the measured gate current. Therefore, the gate current density J_g for HI-EI is written as

$$J_g = J_{leak}(t) + J_{trap}(t) + J_{emit}(t) + J_{sub}(t), \tag{3.1}$$

where $J_{leak}(t)$ is the leakage current component owing to electron and hole flows across the stacked dielectric films, $J_{trap}(t)$ is the displacement current component
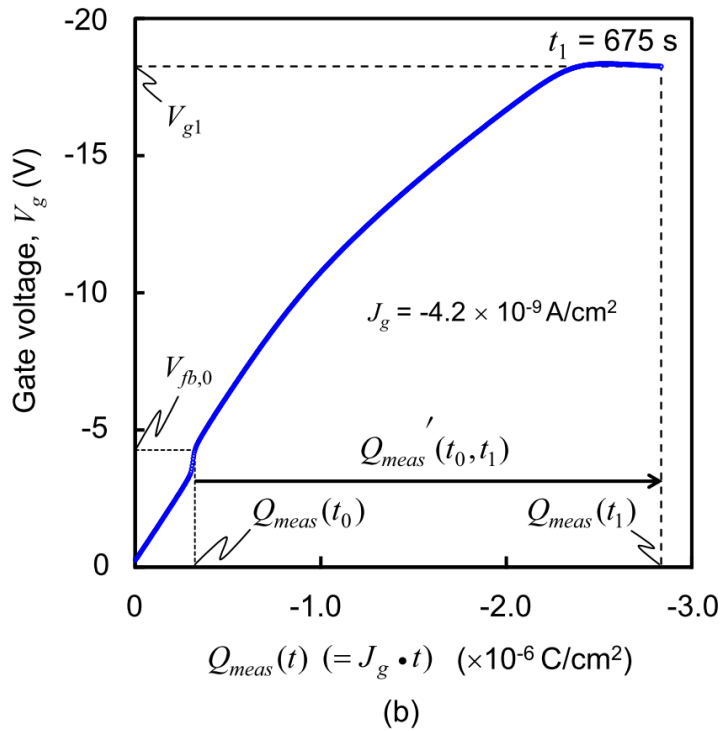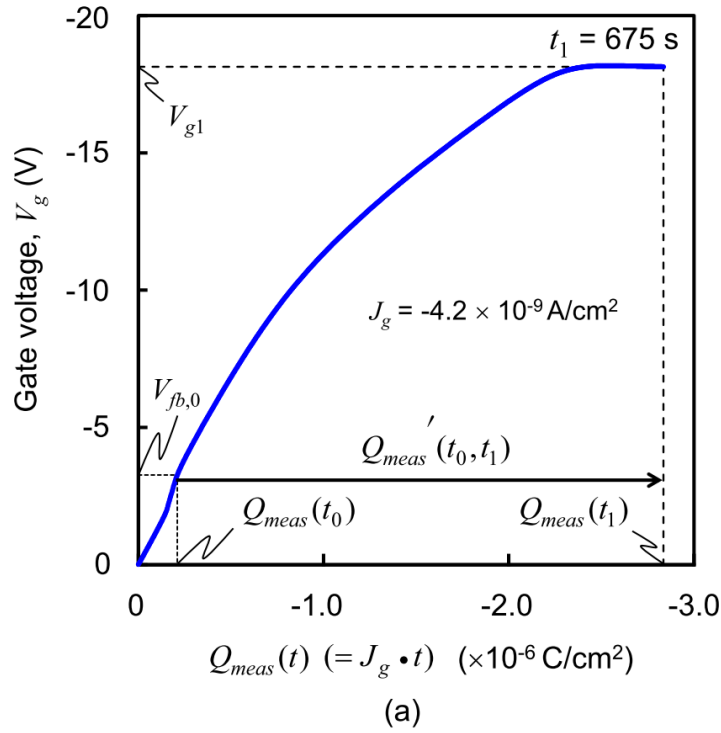
Fig. 3.5 (a) Gate voltage shift as a function of $Q_{meas}(t)$ in the SiCN capacitor during HI-BK. (b) Gate voltage shift as a function of $Q_{meas}(t)$ in the silicon nitride capacitor during HI-BK. Here, $Q_{meas}(t)$ is defined with the gate current density J_g and hole injection time t, as described in Eq. (2.3) in section 2.3.1 in chapter 2. The gate voltage increased monotonously during hole injection.

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owing to hole trapping by trap centers existing in the charge trapping film, $J_{emit}(t)$ the displacement current component owing to electron emission from trap centers and $J_{sub}(t)$ is the displacement current component owing to hole accumulation at the silicon surface. Integration of Eq. (3.1) for the interval t_0 to t_1 in time yields

$$Q_{meas}{}'(t_0,t_1) = Q_{leak}(t_0,t_1) + Q_{trap}(t_0,t_1) + Q_{emit}(t_0,t_1) + Q_{sub}(t_0,t_1). \qquad (3.2)$$

Then, the injected charge per unit area $Q_{inj}(t_0,t_1)$ is defined by

$$Q_{inj}(t_0,t_1) \equiv Q_{leak}(t_0,t_1) + Q_{trap}(t_0,t_1) + Q_{emit}(t_0,t_1) = Q_{meas}{}'(t_0,t_1) - Q_{sub}(t_0,t_1). \qquad (3.3)$$

Here, $Q_{meas}{}'(t_0,t_1)$ and $Q_{sub}(t_0,t_1)$ can be determined by using Eqs. (2.4) and (2.8) explained in section 2.3.1 in chapter 2. Then, F_{inj} for HI-EI is calculated by using the $Q_{inj}(t_0,t_1)$ value discussed above and by using Eq. (2.15) presented in section 2.3.3 in chapter 2. Therefore, in the HI-EI experiment, the F_{inj} value includes the number of emitted electrons per unit area.

3.3.3 Trapping of holes and elimination of trapped electrons in erasing operation

Figure 3.6(a) shows the relationship between $V_{fb,h1}$ and F_{inj} in both the SiCN and silicon nitride memory capacitors subjected to HI-BK and HI-EI. $V_{fb,h1}$ increased with increasing F_{inj}, and then was saturated. At F_{inj} larger than 1.6×10^{13} cm^{-2}, $V_{fb,h1}$ in the HI-EI experiment almost coincided to that in the HI-BK experiment. Figure 3.6(b) shows $V_{fb,h1}$ as a function of F_{inj} in both the silicon nitride memory capacitors subjected to HI-BK and HI-EI. In Fig. 3.6(b), it was also found that $V_{fb,h1}$ in the HI-EI experiment was identical to that in the HI-BK experiment at F_{inj} larger than 1.4×10^{13} cm^{-2}. In the HI-BK experiment, empty trap centers captured holes and created positive charges. In the HI-EI experiment, the same amount of positive charges was created. These results revealed that almost all trapped electrons could not remain in trap centers and were eliminated from the SiCN and silicon nitride films after a large number of holes were injected.

Figure 3.7(a) shows $\Delta V_{fb,h}$ as a function of F_{inj} in the SiCN memory capacitors subjected to HI-BK and HI-EI. $\Delta V_{fb,h}$ in the HI-EI experiment was almost equal to that in the HI-BK experiment when F_{inj} ranged from 0 to 1.0×10^{13} cm^{-2}. On the other hand, $\Delta V_{fb,h}$ for HI-EI was much larger than that for HI-BK at larger F_{inj}. Figure 3.7(b) shows $\Delta V_{fb,h}$ versus F_{inj} in the silicon nitride memory capacitors subjected to HI-BK and HI-EI. In Fig. 3.7(b), while F_{inj} ranged from 0 to 0.8×10^{13} cm^{-2}, $\Delta V_{fb,h}$ was monotonously increased with increasing F_{inj} in both HI-BK and HI-EI experiments and was coincided in both experiments. Additionally, at larger F_{inj}, $\Delta V_{fb,h}$ for HI-EI was larger than that for HI-BK. In Figs, 3.7(a) and 3.7(b), $\Delta V_{fb,h}$ is induced by two events: hole capture by trap centers in the charge trapping films and elimination of electrons trapped in the SiCN and silicon nitride charge trapping films. The presence of the process of electron elimination is responsible for the larger $\Delta V_{fb,h}$ obtained in the HI-EI experiment in both the SiCN and
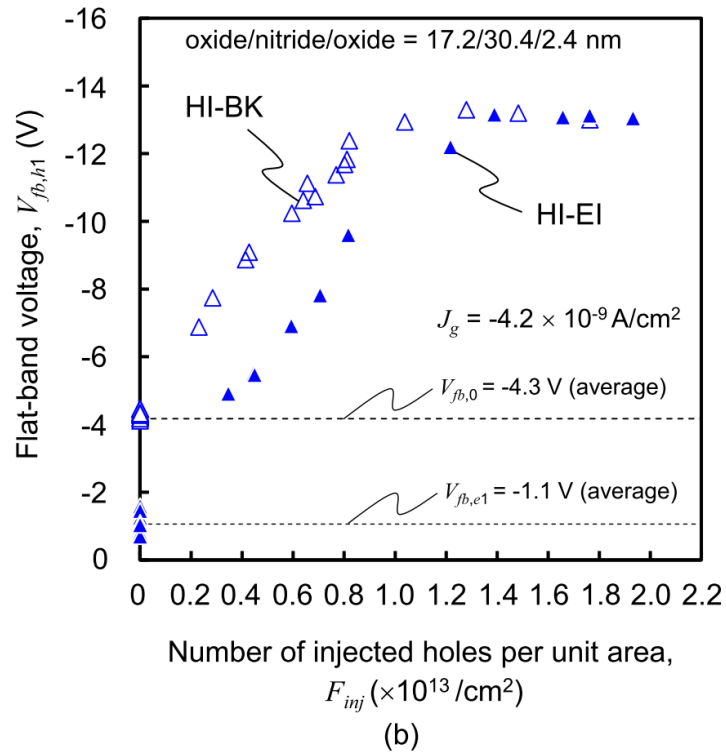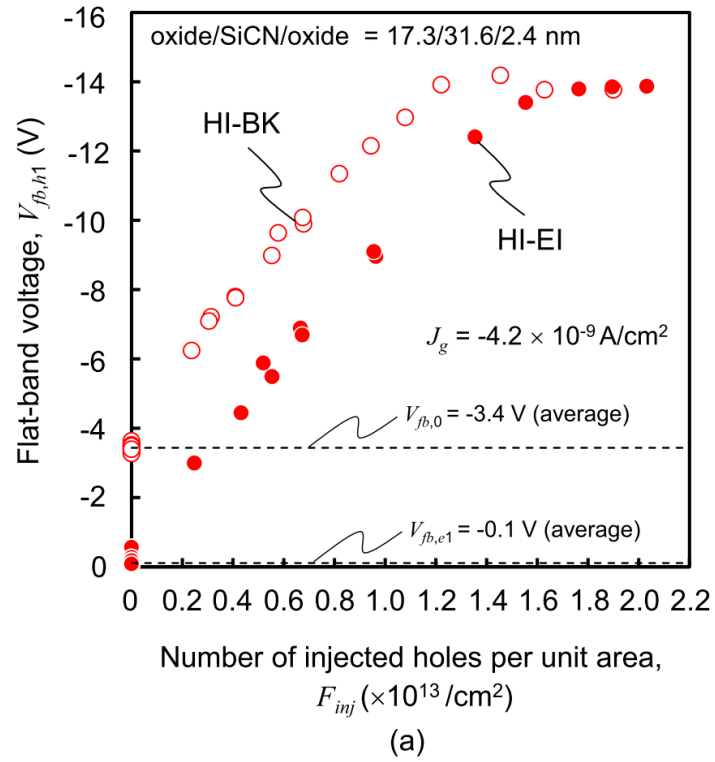
Fig. 3.6 (a) $V_{fb,h1}$ as a function of F_{inj} in the SiCN capacitors subjected to HI-BK and HI-EI. (b) $V_{fb,h1}$ as a function of F_{inj} in the silicon nitride capacitors subjected to HI-BK and HI-EI. Figure 3.6(b) is "Reproduced with permission from ECS Transactions, 75(32), 73 (2017). Copyright 2017, The Electrochemical Society."
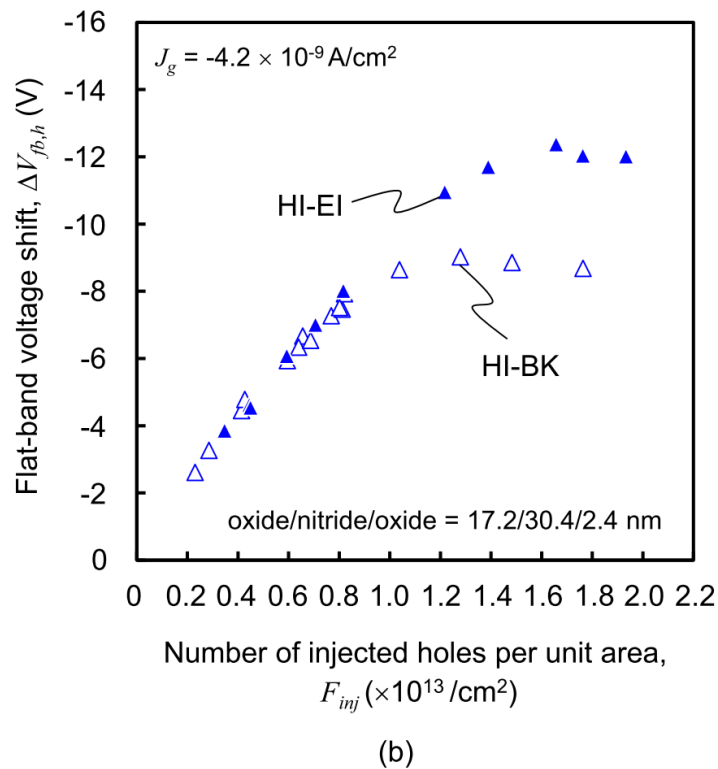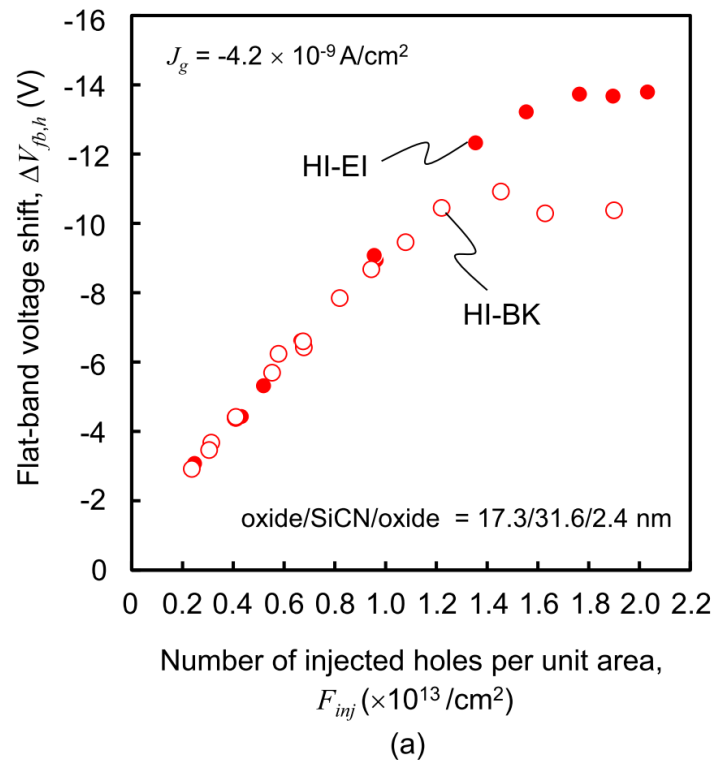
Fig. 3.7 (a) $\Delta V_{fb,h}$ as a function of F_{inj} in the SiCN capacitors subjected to HI-BK and HI-EI. (b) $\Delta V_{fb,h}$ as a function of F_{inj} in the silicon nitride capacitors subjected to HI-BK and HI-EI. Figure 3.7(b) is "Reproduced with permission from ECS Transactions, 75(32), 73 (2017). Copyright 2017, The Electrochemical Society."

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silicon nitride memory capacitors. There are two possible mechanisms for the electron elimination: (i) emission of trapped electrons to the silicon substrate and (ii) recombination of trapped electrons with holes. Further study would be required to determine the mechanism of electron elimination in the charge trapping films.

In Figs, 3.7(a) and 3.7(b), $\Delta V_{fb,h}$ for HI-EI was almost equal to that for HI-BK when F_{inj} ranged from 0 to 1.0×10^{13} cm^{-2}. As described in chapter 2, in the range of small F_{inj} and low gate voltages, $J_{leak}(t)$ is small and $Q_{leak}(t_0, t_1)$ can be neglected in Eq. (2.7) in section 2.3.1. Then, most holes injected to the SiCN and silicon nitride films are captured by trap centers in this range. Therefore, the $\Delta V_{fb,h}$ values in both the HI-BK and HI-EI experiments were determined by F_{inj} values. This resulted in the identical $\Delta V_{fb,h}$ values for HI-BK and HI-EI at small F_{inj}.

In MONOS devices used in the manufacturing industry of NVMs, the thickness of the silicon nitride film is ranging from 3.3 to 12 nm [3-9,12-16]. However, it is difficult to obtain large flat-band voltage shifts in such thin silicon nitride films. On the other hand, thicker charge trapping films with high density of charge trap centers result in the large flat-band voltage shifts of the memory capacitors. As the purpose of this study was to evaluate hole trapping processes in the charge trapping films with both trap centers filled by electrons and empty trap centers. Therefore, in the present study, the thick SiCN and silicon nitride charge trapping films were employed to obtain the clear hole trapping characteristics. Further study would be needed to evaluate the hole trapping characteristics in the thin charge trapping films.

3.4   Conclusions

In this chapter, the hole trapping characteristics of two conditions of the SiCN and silicon nitride films with both trap centers filled by electrons and empty trap centers was studied. In addition, the constant-current carrier injection method was used to investigate the electron elimination phenomena in the SiCN and silicon nitride charge trapping films with trap centers filled by electrons. This method allows to count the number of holes injected to the charge trapping films.

After a large number of holes were injected to the SiCN and silicon nitride films, the flat-band voltage $V_{fb,h1}$ in the memory capacitors with both trap centers filled by electrons and empty trap centers clearly coincided to that with only empty trap centers. This result indicates that almost all electrons trapped in the charge trapping films could not remain in trap centers and could be eliminated after a sufficient number of holes were injected into the films with the trapped electrons. The electrons trapped in the SiCN and silicon nitride films in this study were unstable against holes.

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Chapter 4

Electron retention characteristics of SiCN films for application in charge trapping memories

Chapter 4   Electron retention characteristics of SiCN films for application in charge trapping memories

4.1   Introduction

As described in the previous chapters, nitride-based charge trapping memory, such as the MONOS-type device with an ultrathin tunnel oxide film thinner than 3 nm, has received considerable attention for embedded NVM application due to its several advantages including low programming and erasing voltages, excellent compatibility with the standard CMOS process and better scalability [1-10]. As also introduced in the previous chapters, electrons and holes are captured by trap centers in the silicon nitride charge trapping films during programming and erasing operations, which are applied to store data in the MONOS-type memory cells. As was discussed in chapter 1, the memory cell size in the MONOS-type devices is becoming smaller with rapid downward scaling of NVMs to meet requirements of high capacity and low cost. However, there are some challenges in the MONOS-type devices to achieve the superior performance and reliability. Although alternating charge trapping materials have been explored by several research groups to improve the memory performance and reliability [11-16], no previous studies have been successful in replacing the silicon nitride film.

On the other hand, as mentioned in chapters 1 and 2, Naito *et al*. [17] and Kobayashi *et al*. [18] has intensively studied the application of SiCN films to the charge trapping film of the embedded NVMs. It was reported that the SiCN-based charge trapping memory was found to provide higher programming and erasing speeds than the silicon nitride-based memory [18].

Therefore, the optimization of the alternative materials and the necessity of

overcoming the still existing reliability concerns require an understanding of the charge trap centers distributed in the charge trapping films, which are responsible for the memory effect. To improve data retention characteristics of NVMs, it is important to understand the properties of charge trap centers in the charge trapping films. The long data retention time mainly depends on the spatial distributions and the energy level of the charge trap centers in the band gap of the charge trapping films. In chapter 2, the charge centroid of holes trapped in the SiCN charge trapping films was obtained by using the constant-current carrier injection method. It was found that the charge centroid of trapped holes was initially located near the middle of the films, and then moved to the vicinity of the blocking oxide films with increasing the number of holes injected to the charge trapping films, which is an important information to understand the reliability assurance of the SiCN-based NVM devices. In order to realize the SiCN-based NVMs, it is required to research their charge retention characteristics.

In the previous studies, the emission mechanisms of electrons captured by trap centers in the silicon nitride films have been discussed by several authors [8,19-21]. They have shown that electron tunneling from the trap centers to silicon conduction band (CB) is the dominant emission mechanism at low temperatures (including room temperature). It was also shown that the thermal excitation of electrons from the trap centers to the silicon nitride CB is the dominant mechanism at high temperatures. In both the tunneling and thermal excitation processes, the energy distribution of trap centers filled by electrons would strongly influences the probabilities of electron emission. On the other hand, it has been shown that the SiCN films contain large numbers of hydrogen and carbon atoms [22-24], which might create several kinds of trap centers. Therefore, the understanding of the energy distribution of trap centers in the SiCN films is crucial to achieve sufficient

charge retention time in the SiCN-based memory. However, there are few reports on the energy distribution of trap centers in the SiCN films. In this chapter, an improved analytical method was presented to analyze the emission rate of electrons trapped in the SiCN-based memory capacitors. By using the improved method, the energy distribution of electrons trapped in SiCN charge trapping films was determined.

In this chapter, the charge retention characteristics of the SiCN memory capacitors will be investigated. The formation conditions of samples will first be given in section 4.2. Then, procedures for measuring the charge retention characteristics of the memory capacitors after programming and erasing operations will be explained. In section 4.3, the programming and erasing characteristics of the SiCN memory capacitors will be presented. Then, the charge retention characteristics of the SiCN memory capacitors in programming and erasing conditions at 86 °C will be discussed. Next, to investigate the energy distribution of electrons trapped in the SiCN films, the charge retention characteristics in the programming condition will be presented at four different temperatures. In this chapter, an improved analytical method for the charge retention characteristics in the charge trapping films was presented and the energy distribution of electrons trapped in the SiCN films without any adjustable parameters was extracted. Later, in section 4.3.4, the extracted energy distribution of electrons trapped in the SiCN film will be compared with that in the nitride films. In the last section 4.4, conclusions of this chapter will be delivered.

4.2   Experimental details

4.2.1 Films fabrication

To investigate the charge retention characteristics, memory capacitors with a blocking oxide-SiCN-tunnel oxide stacked film structure were fabricated on p-type (100) silicon substrates. A schematic cross section of the memory capacitors is shown in Fig. 4.1. Table 4.1 shows the summary of the formation conditions of the samples. First, a 2.4-nm-thick tunnel oxide film was formed by a rapid thermal oxidation of the silicon substrates. Then, a 31.5-nm-thick SiCN film as the charge trapping film was formed by a PECVD using $Si(CH_3)_4$ and NH_3 gases at 400 °C. After the charge trapping film was formed, a blocking oxide film of 17.3 nm in thickness was grown using a PECVD technique. Finally, an aluminum film was deposited by a thermal evaporation technique to form the gate electrodes on the oxide-SiCN-oxide stacked films. The gate area of the memory capacitors was $1.1 \times 10^{-2}\, cm^2$. The refractive index of the SiCN film was found to be 1.91 at a wavelength of 632.8 nm using a spectroscopic ellipsometer (SOPRA MOSS-ES4G). The static relative dielectric constant of the SiCN film was determined to be 4.8 from capacitance measurements.

As was presented in chapter 2, XPS measurements were performed to investigate the elemental composition of the SiCN film. Depth profiles of each element in the film were collected after every 1-min sputtering using a 1 kV Ar ion beam. The atomic ratios of N and C to Si of the SiCN film were obtained to be 0.41 ± 0.04 and 0.77 ± 0.06, respectively. The atomic ratios were found to be nearly constant throughout the thickness of the SiCN film. In addition, the surface roughness of the SiCN, blocking oxide, and tunnel oxide single-layer films was measured by AFM. It was found that the film surfaces were smooth

with the estimated roughness values of R_a and R_q below 0.3 nm, which lead to confirm the surface quality of the films in evaluating the charge retention characteristics of the memory capacitors with the blocking oxide-SiCN-tunnel oxide stacked films structure.

V_g = +14.3 V or -15.1 V

Aluminum electrode

Blocking oxide film, 17.3 nm

SiCN charge trapping film, 31.5 nm

Tunnel oxide film, 2.4 nm

p-type (100) silicon substrate
9-12 Ωcm
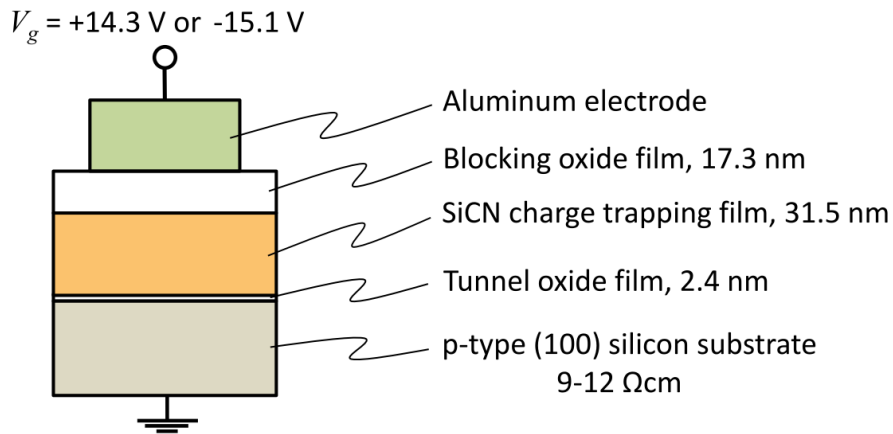
Fig. 4.1 Schematic cross section of test capacitors with an aluminum electrode-blocking oxide-SiCN-tunnel oxide-silicon structure. (Copyright 2017 IEICE, [Sheikh Rashel Al AHMED and Kiyoteru KOBAYASHI, Extraction of Energy Distribution of Electrons Trapped in Silicon Carbonitride (SiCN) Charge Trapping Films, IEICE TRANS. ELECTRON., 2017, Vol. E100-C, No. 7, pp. 662-668] Fig. 1)

Table 4.1 Summary of the formation conditions of the samples.

Film	Thickness (nm)	Refractive index	Method	Temperature (°C)	Source gases
Blocking oxide	17.3	1.48	PECVD	400	SiH_4+N_2O
SiCN	31.5	1.91	PECVD	400	$Si(CH_3)_4+NH_3$
Tunnel oxide	2.4	1.46	Thermal oxidation	1050	

4.2.2 Procedures for measuring charge retention characteristics

After the sample fabrication, the samples were placed in an oven chamber. All the memory capacitors were baked in the air at 235 °C to emit electrons and holes trapped in the stacked dielectric films. The 235 °C baking and measurements of the capacitance-voltage (CV) characteristics were conducted alternately and it was confirmed that the flat-band voltage $V_{fb,0}$ converged to a value of -3.1 V. The total baking time was 1.2×10^6 s. The CV characteristics were measured at 100 kHz with an Agilent E4980A LCR meter. To turn the SiCN memory capacitors into programming or erasing condition, a programming voltage of +14.3 V or an erasing voltage of -15.1 V was applied to the gate electrode. The programming and erasing voltages were applied by using an Agilent 33210A function generator. In order to maintain an inversion condition in the p-type silicon substrates under the positive gate bias, the memory capacitors were exposed to visible light during the programming operation. The charge retention characteristics in programming condition were measured at four different temperatures ranging from 23 to 235 °C. The charge retention characteristics in erasing condition were also measured at 86 °C. Figure 4.2 shows the procedures to measure the charge retention characteristics after the programming and erasing conditions.

Programming condition

● Baking the capacitors at 235 °C
   CV measurement was conducted to determine flat-band voltage $V_{fb,0}$

○ Programming voltage, V_g = +14.3 V
   Electrons were trapped.

○ Erasing voltage, V_g = -15.1 V
   Holes were trapped.

● Programming voltage, V_g = +14.3 V
   Electrons were trapped.

○ CV measurement
   Flat-band voltage V_{fb} was determined.

● Room temperature (23 °C) and 86 °C, 160 °C, 235 °C baking

○ CV measurement
   Flat-band voltage shift ΔV_{fb} was determined after room temperature and baking at high temperatures.
   ($\Delta V_{fb} = \Delta V_{th}$)

Erasing condition

● Baking the capacitors at 235 °C
   CV measurement was conducted to determine $V_{fb,0}$

○ Programming voltage, V_g = +14.3 V
   Electrons were trapped.

● Erasing voltage, V_g = -15.1 V
   Holes were trapped.

○ CV measurement
   Flat-band voltage V_{fb} was determined.

● 86 °C baking

○ CV measurement
   Flat-band voltage shift ΔV_{fb} was determined after room temperature and baking at high temperatures.
   ($\Delta V_{fb} = \Delta V_{th}$)

Fig. 4.2 Procedures to measure the charge retention characteristics after the programming and erasing conditions.

4.3   Results and discussion

4.3.1 Capacitance-voltage characteristics of SiCN memory capacitor

Figure 4.3 shows the CV characteristics of the SiCN memory capacitor before and after the baking at 235 °C, after the programming operation, and during the charge retention test at 86 °C. To empty all trap centers existing in the SiCN charge trapping film, the capacitor was baked at 235 °C. The $V_{fb,0}$ value was obtained to be -3.1 V by analyzing the CV curve of the baked capacitor. After a programming voltage of +14.3 V was applied to the gate electrode with grounded silicon substrate, the CV curve was shifted toward the positive voltage direction. This shift indicates that a negative charge was accumulated in the SiCN memory capacitor.
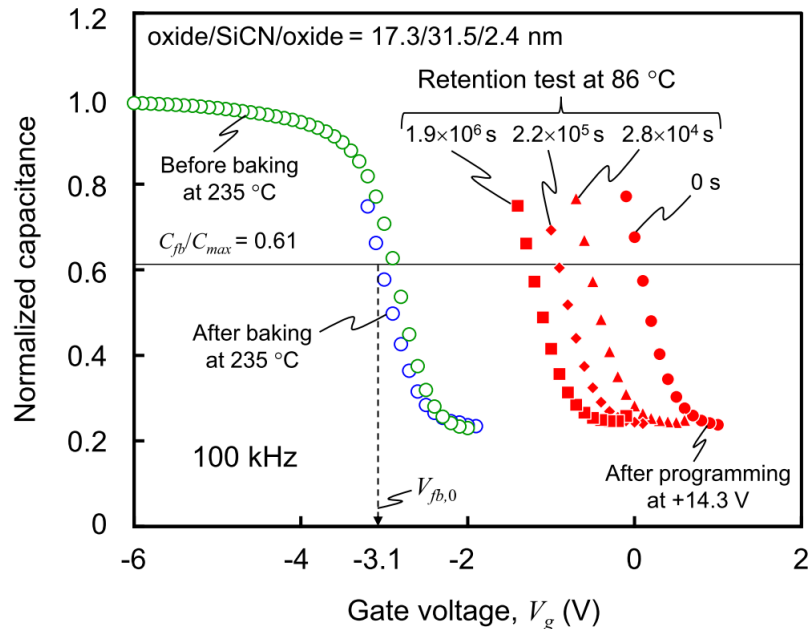
Fig. 4.3 CV characteristics of the memory capacitors with the blocking oxide-SiCN-tunnel oxide stacked films. (Copyright 2017 IEICE, [Sheikh Rashel Al AHMED and Kiyoteru KOBAYASHI, Extraction of Energy Distribution of Electrons Trapped in Silicon Carbonitride (SiCN) Charge Trapping Films, IEICE TRANS. ELECTRON., 2017, Vol. E100-C, No. 7, pp. 662-668] Fig. 2)

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4.3.2 Programming and erasing characteristics of SiCN memory capacitors

Figure 4.4 shows the programming and erasing characteristics of the SiCN memory capacitors. As mentioned in the section 4.2.2, the programming voltage of +14.3 V was applied to the gate electrode with grounded silicon substrate to turn the SiCN memory capacitor into the programming condition. After the programming operation, the flat-band voltage was varied toward the positive voltage direction. Following the programming operation, the gate electrode was negatively biased at -15.1 V. In Fig. 4.4, after the erasing operation, the flat-band voltage was shifted toward the negative voltage direction. This shift is attributed due to a positive charge accumulation in the memory capacitor. A memory window of 6.9 V was obtained. These results show that electrons and holes were injected into the SiCN film from the silicon substrate through the thin tunnel oxide film via the quantum mechanical tunneling under the positive and negative gate bias and some of the injected electrons and holes were trapped in the SiCN charge trapping film.
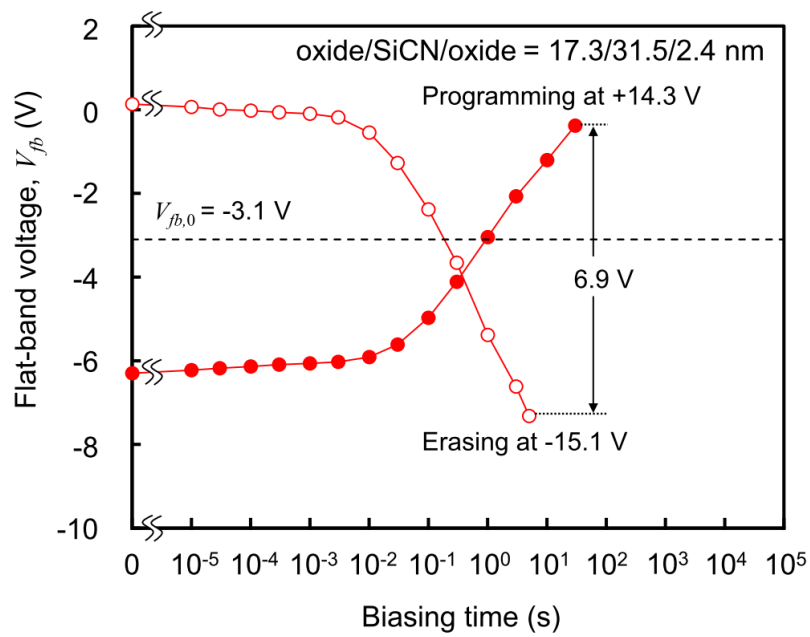
Fig. 4.4 Programming and erasing characteristics of the SiCN memory capacitors. The thicknesses of the blocking oxide, SiCN, and tunnel oxide films were 17.3, 31.5, and 2.4 nm, respectively.

4.3.3 Charge retention characteristics of SiCN memory capacitors at 86 °C

To measure the charge retention characteristics, the baking and measurements of the CV characteristics were alternately carried out after the programming and erasing operations. In Fig. 4.3, after the programming operation, the CV curve of the SiCN memory capacitor baked at 86 °C was shifted toward the negative voltage direction. The flat-band voltage was obtained by analyzing the CV curves of the baked capacitor. Figure 4.5 shows the charge retention characteristics of the SiCN memory capacitors in programming and erasing conditions at 86 °C. The testing temperature nearly equaled the maximum operating temperature of 85 °C which is typically required for NVM-embedded micro computing units. As mentioned in the section 4.2.2, the flat-band voltage $V_{fb,0}$ was determined to be -3.1 V by analyzing the CV curves of the baked capacitors. After the programming operation and the subsequent retention test at 86 °C, the flat-band voltage was shifted toward $V_{fb,0}$. This shift is mainly due to the emission of electrons from the trap centers. In the erasing condition in Fig. 4.5, the flat-band voltage was also shifted toward $V_{fb,0}$. This shift is mainly due to hole emission from the trap centers. The initial memory window of 6.4 V was stored in the SiCN memory capacitors before the retention test at 86 °C. After ten years retention at 86 °C, the remaining memory window of the SiCN memory capacitors was roughly estimated to be 25 % of the initial memory window. The result leads us to suggest that the SiCN dielectric films can be utilized as the charge trapping film of embedded NVMs.
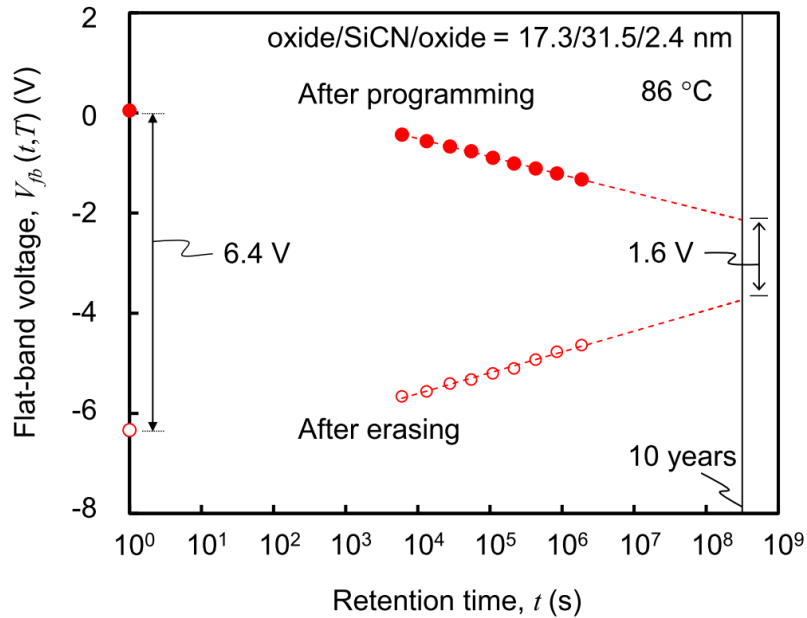
Fig. 4.5 Charge retention characteristics of the SiCN memory capacitors in programming and erasing conditions at 86 °C. The testing temperature nearly equaled the maximum operating temperature of 85 °C which is typically required for NVM-embedded micro computing units. The remaining memory window of the SiCN memory capacitors after ten years was roughly estimated to be 25 % of the initial memory window. (Copyright 2017 IEICE, [Sheikh Rashel Al AHMED and Kiyoteru KOBAYASHI, Extraction of Energy Distribution of Electrons Trapped in Silicon Carbonitride (SiCN) Charge Trapping Films, IEICE TRANS. ELECTRON., 2017, Vol. E100-C, No. 7, pp. 662-668] Fig. 4)

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4.3.4 Extraction of energy distribution of trapped electrons

To investigate the energy distribution of electrons trapped in the SiCN films, the charge retention characteristics in the programming condition were measured at four different temperatures. Figure 4.6(a) shows the flat-band voltage versus retention time. The flat-band voltage shift at a fixed retention time was larger for the higher testing temperature.

Assuming that the trapped electrons have a spatially uniform distribution in the SiCN film, the number of filled trap centers per unit volume at retention time t for the testing temperature T, $N(t,T)$, has a relationship with the following expression:

$$N(t,T) \propto V_{fb}(t,T) - V_{fb,0},$$ (4.1)

where $V_{fb}(t,T)$ is the flat-band voltage at retention time t for the testing temperature T. Then, the occupancy function $f(t,T)$ is defined as the form

$$f(t,T) \equiv \frac{N(t,T)}{N(0,T)} = \frac{V_{fb}(t,T) - V_{fb,0}}{V_{fb}(0,T) - V_{fb,0}}.$$ (4.2)

Figure 4.6(b) shows $f(t,T)$ versus retention time t for the SiCN memory capacitors at different temperatures. The electron emission rate $df(t,T)/d\log t$ was larger for the higher testing temperature.

Several authors have analyzed the energy distribution of electrons trapped in the silicon nitride charge trapping films [8,19-21]. Lundkvist *et al*. presented a theoretical model to explain the retention characteristics of MNOS devices [19]. It needed two adjustable parameters, such as the mean free path for direct tunneling of electrons λ and inverse of the attempt-to-escape frequency τ_e, to derive the energy distribution. The model based on thermal excitation of charge carriers from trap centers was proposed by
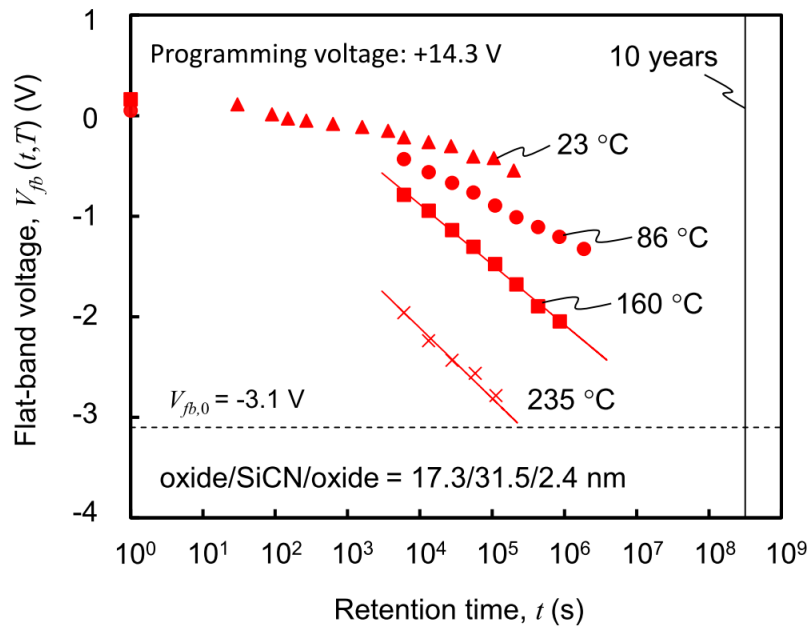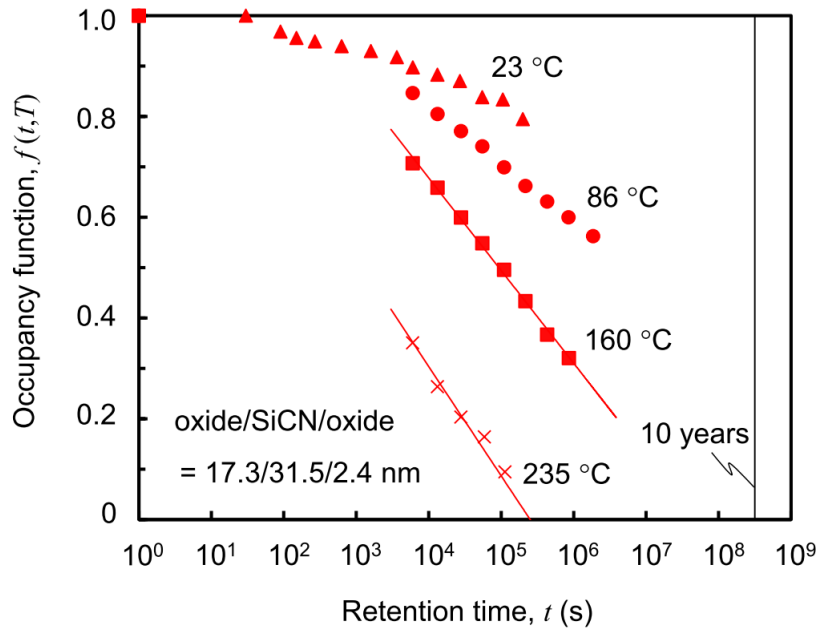
Fig. 4.6 (a) Variations in the flat-band voltage at four different temperatures in the SiCN memory capacitors. The flat-band voltage shift at a fixed retention time was larger for the higher testing temperature. (b) Occupancy function $f(t,T)$ versus retention time t at different temperatures. The electron emission rate $\mathrm{d}f(t,T)/\mathrm{d}\log t$ was larger for the higher testing temperature.

McWhorter *et al.*. It also needed two adjustable parameters of λ and the capture cross-section of electron trap centers σ to analyze the nitride trap distribution in energy [20]. Wang and White derived an analytical retention model based on the trap-to-band tunneling and thermal excitation mechanisms for electron emission [8]. They assumed a value of σ to determine the energy distribution of trapped electrons. Arreghini *et al.* presented an improved model for electron emission from trap centers, which required σ and the effective masses of electrons in silicon oxide and in silicon nitride films, m_{ox} and m_n [21,25,26]. It should be noted that a set of parameters, such as λ, τ_e, σ and m_n, of the silicon nitride films were needed in the previous analytical models to determine the energy distribution of trap centers. However, there has been no report concerning the appropriate values of these parameters for the SiCN films. To discuss the energy distribution of electrons trapped in the SiCN films numerically from the experimental results shown in Fig. 4.6(b), an improved method is presented which needs no adjustable and extra parameters in the following paragraphs.

Figures 4.7(a) and 4.7(b) show the schematic energy band diagram and the energy distribution of electrons trapped in the charge trapping film. In Fig. 4.7(b), vertical axis is defined as the trap depth Φ_E from the bottom of the CB. The trap centers filled by electrons are assumed to be range from Φ_{EH} to Φ_{EL} in the forbidden gap of the charge trapping film, as shown in Fig. 4.7(a), and that the energy distribution of the filled trap centers is uniform in the range, as shown in Fig. 4.7(b). Trapped electrons are emitted in ascending order of the trap depth by thermal excitation during the retention test, as shown in Fig. 4.7(c). In Fig. 4.7(d), the energy distribution of trap centers filled by electrons after a period of retention time is represented by solid line. Then, the $N(t,T)$ is given by
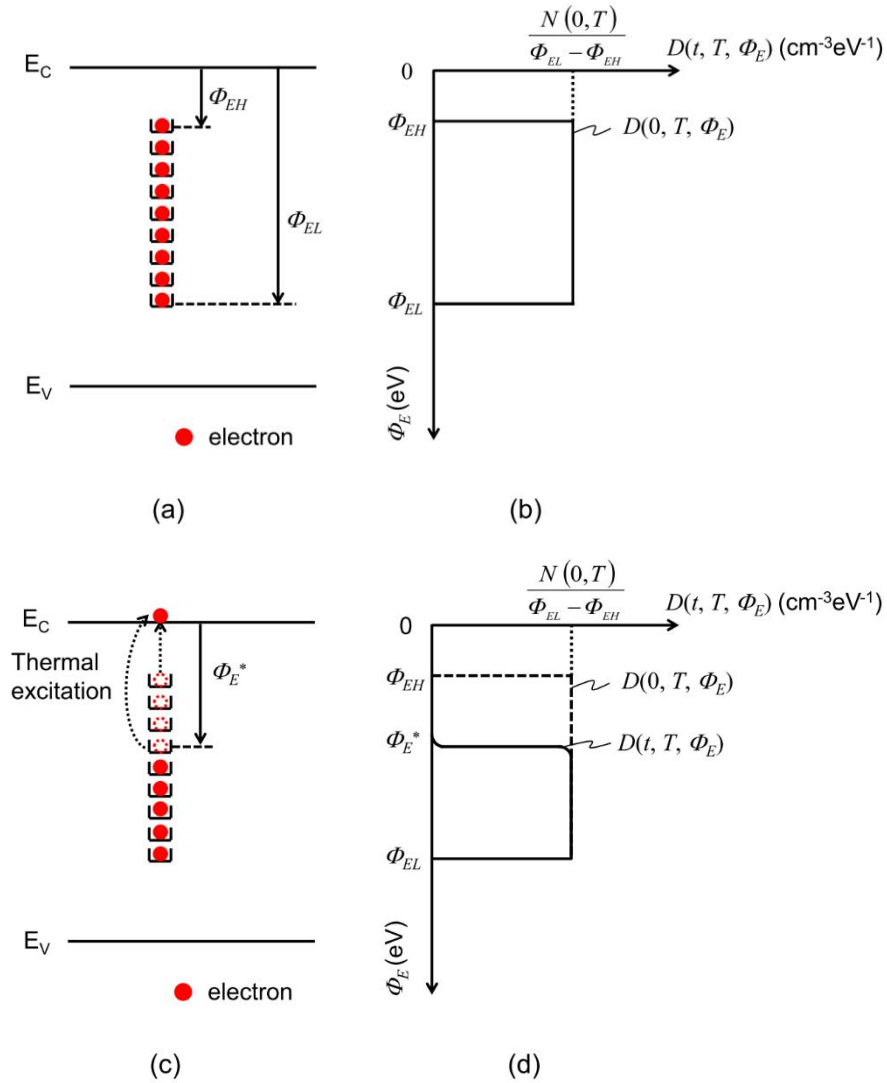
Fig. 4.7 Schematic representations of the energy distribution of electrons trapped in the SiCN band gap. (a) The energy band diagram and the energy distribution of electron trap centers of the SiCN film. (b) A uniform energy distribution of the electron trap centers inside the SiCN film is assumed. (c) Trapped electrons are emitted in ascending order of trap depth by thermal excitation during the retention test. (d) The energy distribution of electron trap centers after a period of retention time. (Copyright 2017 IEICE, [Sheikh Rashel Al AHMED and Kiyoteru KOBAYASHI, Extraction of Energy Distribution of Electrons Trapped in Silicon Carbonitride (SiCN) Charge Trapping Films, IEICE TRANS. ELECTRON., 2017, Vol. E100-C, No. 7, pp. 662-668] Fig. 6)

$$N(t,T) = \int_0^{\Phi_{EL}} D(t,T,\Phi_E)\,d\Phi_E , \qquad (4.3)$$

where $D(t,T,\Phi_E)$ is the number of the filled trap centers per unit volume and unit

energy. The first order rate equation for the change of $D(t,T,\Phi_E)$ can be given in the

form

$$\frac{\partial}{\partial t} D(t,T,\Phi_E) = -\frac{1}{\tau(T,\Phi_E)} D(t,T,\Phi_E),$$ (4.4)

where $\tau(T,\Phi_E)$ is the time constant of thermal excitation of electrons. Solving Eq. (4.4), we have

$$D(t,T,\Phi_E) = D(0,T,\Phi_E)\exp\left[-\frac{t}{\tau(T,\Phi_E)}\right].$$ (4.5)

The time constant $\tau(T,\Phi_E)$ is assumed to follow Boltzmann statistics:

$$\tau(T,\Phi_E) = \tau_0 exp\left(\frac{\Phi_E}{k_B T}\right),$$ (4.6)

where τ_0 is the pre-exponential coefficient. Substituting Eqs. (4.3) and (4.5) into Eq. (4.2) yields

$$f(t,T) = \frac{N(t,T)}{N(0,T)}$$

$$= \frac{1}{N(0,T)} \int_0^{\Phi_{EL}} D(0,T,\Phi_E)\exp\left[-\frac{t}{\tau(T,\Phi_E)}\right]d\Phi_E.$$ (4.7)

Here, the following approximation [8,19-21] is used

$$\exp\left[-\frac{t}{\tau(T,\Phi_E)}\right] \approx \begin{cases} 0 & \Phi_E < \Phi_E{}^* \\ 1 & \Phi_E \geq \Phi_E{}^* \end{cases},$$ (4.8)

where

$$\Phi_E{}^* = k_B T \ln\left(\frac{t}{\tau_0}\right).$$ (4.9)

Thus, the following simple form from Eqs. (4.5) and (4.7) is obtained,

$$f(t,T) \approx \frac{\Phi_{EL} + k_B T \ln \tau_0}{\Phi_{EL} - \Phi_{EH}} - \frac{k_B T}{\Phi_{EL} - \Phi_{EH}} \ln t$$

$$= \frac{\Phi_{EL} + 2.30 k_B T \log \tau_0}{\Phi_{EL} - \Phi_{EH}} - \frac{2.30 k_B T}{\Phi_{EL} - \Phi_{EH}} \log t.$$ (4.10)

From Eq. (4.10), the electron emission rate $\mathrm{d}f(t,T)/\mathrm{d}\log t$ can be written as

$$\frac{\mathrm{d}f(t,T)}{\mathrm{d}\log t} = -\frac{2.30 k_B}{\Phi_{EL} - \Phi_{EH}} T \ . \tag{4.11}$$

As shown in Fig. 4.6(b), the occupancy function $f(t,T)$ obtained from the retention tests at high temperatures 160 and 235 °C followed linear functions of $\log t$. This fact supports the validity of Eq. (4.10). Figure 4.8 shows the electron emission rate $\mathrm{d}f(t,T)/\mathrm{d}\log t$ as a function of T. According to Eq. (4.11), $\mathrm{d}f(t,T)/\mathrm{d}\log t$ is zero at $T = 0$ K. In Fig. 4.8, the $\mathrm{d}f(t,T)/\mathrm{d}\log t$ values of retention tests at 160 and 235 °C followed a linear function of the testing temperature T passing through the origin. This result leads us to suggest that the thermal excitation of electrons from the trap centers is the dominant mechanism for the electron emission at the high temperatures.
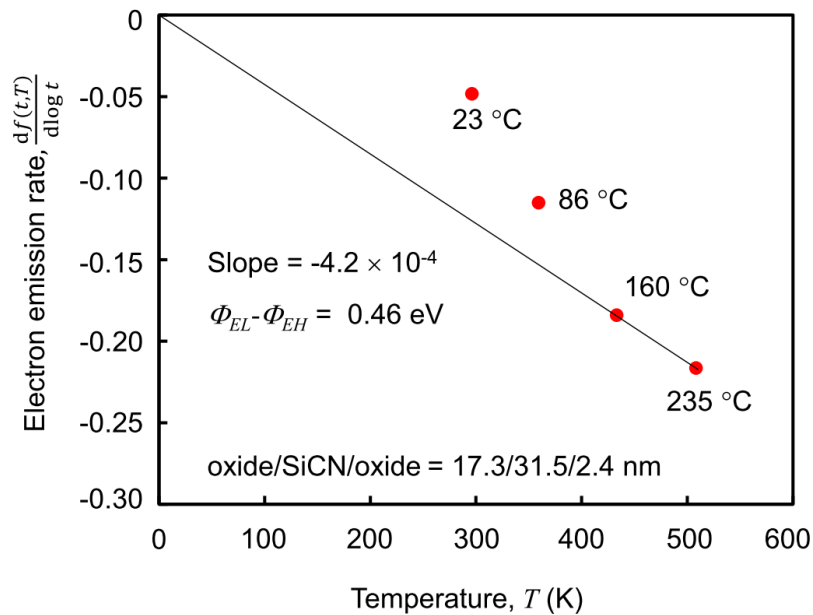
Fig. 4.8 Electron emission rate $\mathrm{d}f(t,T)/\mathrm{d}\log t$ as a function of the testing temperature T for the SiCN memory capacitors. According to Eq. (4.11), $\mathrm{d}f(t,T)/\mathrm{d}\log t$ is zero at $T = 0$ K. The $\mathrm{d}f(t,T)/\mathrm{d}\log t$ values of retention tests at 160 and 235 °C followed a linear function of the testing temperature T passing through the origin. (Copyright 2017 IEICE, [Sheikh Rashel Al AHMED and Kiyoteru KOBAYASHI, Extraction of Energy Distribution of Electrons Trapped in Silicon Carbonitride (SiCN) Charge Trapping Films, IEICE TRANS. ELECTRON., 2017, Vol. E100-C, No. 7, pp. 662-668] Fig. 7)

In Fig. 4.8, the d$f(t,T)$/dlog t values of the retention tests at 23 and 86 °C did not follow a linear function of the testing temperature T. The electron emission in the charge retention tests at the low temperatures is dominated by the electron tunneling from the trap centers to the CB of silicon [8]. On the other hand, the proposed analytical method is based on the thermal excitation mechanism. Therefore, the proposed method can not be used to analyze the test results at 23 and 86 °C, which do not follow Eq. (4.11).

On the basis of Eq. (4.11), a value of $\Phi_{EL} - \Phi_{EH}$ was determined to be 0.46 eV from the slope of the d$f(t,T)$/dlog t-T plot shown in Fig. 4.8. By combining the intercepts of the $f(t,T)$-log t plots for the 160 and 235 °C test results in Fig. 4.6 (b) and the first term in Eq. (4.10), the following two equations can be derived:

$$\frac{\Phi_{EL} + 2.30 k_B \times (433.15) \times \log \tau_0}{0.46} = 1.41 \quad \text{for 160 °C} \tag{4.12a}$$

and

$$\frac{\Phi_{EL} + 2.30 k_B \times (508.15) \times \log \tau_0}{0.46} = 1.17 \quad \text{for 235 °C.} \tag{4.12b}$$

Solving Eqs. (4.12a) and (4.12b), Φ_{EL} and τ_0 were obtained to be 1.3 eV and 2.8×10^{-8} s. Thus, as shown in Fig. 4.9, the electron trap centers were determined to be distributed from 0.8 to 1.3 eV below the CB edge in the SiCN film without using any adjustable parameters.

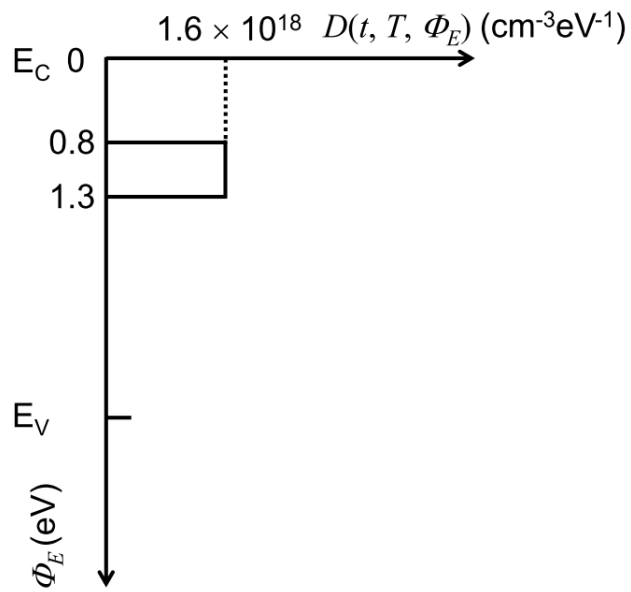**Fig. 4.9** Energy distribution of electrons trapped in the SiCN charge trapping film. Energy distribution of trapped electrons was extracted to be from 0.8 to 1.3 eV below the conduction band edge in the SiCN film without using any adjustable parameters.

4.3.5 Comparisons of energy depth of electrons trapped in SiCN and nitride films

Several studies for the MONOS devices have reported the energy distribution of electrons trapped in silicon nitride and oxynitride films grown by using LPCVD techniques. According to Aozasa and co-workers, the energy level of electron trap centers was located at 0.8-0.9 eV below the CB edge in a silicon nitride film which was deposited from the SiH_2Cl_2-NH_3 system at 680 °C by LPCVD [27]. Wang and White extracted a broad distribution of trapped electrons ranging from 0.6 to 2.1 eV below the CB edge in an oxynitride film [8]. Arreghini *et al.* also reported that the electron trap centers were distributed from 0.6 to 1.2 eV below the CB edge in a standard LPCVD silicon nitride film [21]. The energy depth of electrons trapped in the SiCN film, which was obtained to range from 0.8 to 1.3 eV below the CB edge in the present work, is comparable with that in the silicon nitride and oxynitride films. As discussed in the section 4.3.3, the electron retention characteristics at high temperatures are dominated by the trap depth. Therefore, it is suggested that the SiCN dielectric film is a potential candidate which can replace silicon nitride film as the charge trapping film.

In the previous study, it was reported that the erasing speed in the SiCN-based charge trapping memory was higher than that in the silicon nitride-based memory [18]. As was discussed in chapter 1, the erasing operation is mainly dominated by the three mechanisms: hole injection from silicon to charge trapping film, hole trapping in the charge trapping film and electron emission from the film. The electron emission speed depends on the probability of electron tunneling from electron trap centers to the CB of silicon. The energy barrier height for the electron tunneling is determined by the sum of the energy depth of electron trap centers and the CB offset at the SiCN-tunnel oxide interface. Therefore, the energy depth of electron trap centers is one of the parameters

dominating the erasing speed, which was comparable in the SiCN and silicon nitride films. On the other hand, as mentioned above, the hole injection and hole trapping are also the dominant mechanisms in the erasing operation. To explain the higher erasing speed in the SiCN-based memory, further study on the hole injection and hole trapping mechanisms would be required.

4.4 Conclusions

The charge retention characteristics of memory capacitors with blocking oxide-SiCN-tunnel oxide stacked films were investigated. In the charge retention test at 86 °C, the charge retention time of more than 10 years was estimated for the SiCN capacitors.

To analyze the energy distribution of electrons trapped in the new dielectric films, an improved analytical method was presented in this study. Using the improved method, the energy distribution of electrons trapped in the SiCN charge trapping films was extracted numerically. The method allows the extraction of energy level of electron trap centers in the SiCN band gap with no adjustable parameters. The electrons trapped in the SiCN film during programming at 14.3 V were found to be distributed from 0.8 to 1.3 eV below the conduction band edge. It is suggested that the presence of such deep trap centers in the SiCN films results in the long data retention time in the SiCN-based memories. Hence, the SiCN dielectric film is a potential candidate which can replace silicon nitride film as the charge trapping film of embedded NVMs.

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Chapter 5

Summary and future works

Chapter 5   Summary and future works

5.1   Summary

The metal-oxide-nitride-oxide-semiconductor (MONOS)-type memory device with an ultrathin tunnel oxide film has attracted considerable attention for embedded nonvolatile memory (NVM) applications. Electron and hole trapping phenomena in silicon nitride film induce shifts in the threshold voltage of memory transistors, which are applied to programming and erasing operations in the MONOS devices. The memory cell size in the MONOS-type devices has been becoming smaller in the past few decades. In such small memory cells, it is a challenge to promote the programming and erasing speeds and data retention simultaneously. In this dissertation, to get a better understanding of the charge trapping mechanisms in programming and erasing operations, the constant-current carrier injection method was proposed. Recently, silicon carbonitride (SiCN) dielectric film has been expected to be a new charge trapping film of embedded NVMs instead of the silicon nitride film. Therefore, the proposed method was used to investigate the hole trapping characteristics of memory capacitors with blocking oxide-SiCN-tunnel oxide and blocking oxide-silicon nitride-tunnel oxide stacked films. The charge centroid of holes captured by only empty trap centers in the SiCN and silicon nitride charge trapping films was extracted by using the proposed method. The proposed constant-current carrier injection method was also used to investigate the electron elimination phenomena in the SiCN and silicon nitride charge trapping films with trap centers filled by electrons. In addition, an improved analytical method was presented, which allows the extraction of energy distribution of carriers trapped in the SiCN or new dielectric films with no adjustable parameters. This dissertation consists of five chapters. The contents of each

chapter are summarized as follows.

In chapter 1, an overview of the MONOS-type memory devices was firstly introduced. Next, a brief explanation of the requirements for NVMs was given. The influence of the properties of the charge trap centers on the performance and reliability of NVMs was mentioned also. The research background of the application of the SiCN film to the charge trapping film in NVMs was presented. Then, the objectives of this dissertation were given. Finally, the organization of the dissertation was described.

In chapter 2, the constant-current carrier injection method was proposed to analyze the charge centroid of carriers trapped in stacked dielectric films and to count the number of carriers injected to the stacked films. The charge centroid of holes trapped in the SiCN and silicon nitride charge trapping films with only empty trap centers was extracted by using the proposed method.

In order to investigate the uniformity of elemental compositions in the blocking oxide-SiCN-tunnel oxide and the blocking oxide-silicon nitride-tunnel oxide stacked films, X-ray photoelectron spectroscopy (XPS) measurements were performed. It was found that the atomic ratios of N, C, and O to Si were nearly constant throughout the thickness of the blocking oxide, SiCN, and silicon nitride films. In addition, the surface roughness of the SiCN, silicon nitride, blocking oxide, and tunnel oxide single-layer films was investigated by atomic force microscopy (AFM) technique. It was found that the surface of the fabricated films was smooth with the arithmetic mean roughness (R_a) and root-mean-square roughness (R_q) below 0.3 nm. The estimated small roughness values lead us to confirm the surface quality of the SiCN, silicon nitride, blocking oxide, and tunnel oxide films in evaluating the charge centroid of these films.

In this chapter, the extraction method of the charge centroid of trapped carriers in the memory capacitors subjected to the constant-current carrier injection was explained in detail. The leakage current in the stacked dielectric films was also analyzed. Then, the experimental results of the charge centroid of holes trapped in the SiCN and silicon nitride films after the constant-current hole injection were presented. It was found that the charge centroid of holes captured by only empty trap centers was initially located near the middle of the SiCN and silicon nitride films, and then moved toward the blocking oxide-SiCN interface or the blocking oxide-silicon nitride interface with increasing the number of injected holes per unit area F_{inj}. It was also found that the charge centroid in the SiCN film was closer to the blocking oxide film as compared to that in the silicon nitride film. The location of the charge centroid in the SiCN film was explained by the model that holes were easily transported toward the blocking oxide-SiCN interface because of the high electric field, the low dynamic dielectric constant and the presence of the shallow trap centers involved in the Poole-Frenkel (PF) conduction in the SiCN film.

In this chapter, the charge centroid of holes trapped in the SiCN and silicon nitride charge trapping films with only empty trap centers was extracted by using the constant-current carrier injection method. The proposed method enables us to count the number of carriers injected to the stacked films and provides the accurate estimation of the charge centroid of trapped carriers. The charge centroid is an important information for understanding the carrier trapping mechanism in the programming and erasing operations of NVMs.

In chapter 3, the electron elimination phenomena in the SiCN and silicon nitride charge trapping films with trap centers filled by electrons was investigated by using the

constant-current carrier injection method.

In this chapter, the measurement procedures of the hole trapping characteristics of the two conditions were introduced. After a negative gate voltage was applied, the capacitance-voltage (CV) measurements were performed to determine the flat-band voltage shift in the SiCN and silicon nitride memory capacitors of the two conditions. Next, the constant-current carrier injection method was used to investigate the hole trapping characteristics quantitatively in the memory capacitors. This method allows to count the number of holes injected to the charge trapping films both trap centers filled by electrons and only empty trap centers. Then, the hole trapping and electron elimination in the erasing operation of the SiCN and silicon nitride memory capacitors were discussed. It was found that the flat-band voltages in the memory capacitors with both trap centers filled by electrons and empty trap centers coincided to that with only empty trap centers after a large number of holes were injected into the charge trapping films. This result indicates that almost all trapped electrons could not remain in trap centers and were eliminated from the SiCN and silicon nitride films under negative gate bias.

In chapter 4, an improved analytical method for the charge retention characteristics in the charge trapping films was presented. This method allows the extraction of energy level of electrons trapped in the SiCN or new dielectric films with no adjustable parameters. In the present study, the electron trap centers were determined to be distributed from 0.8 to 1.3 eV below the conduction band edge in the SiCN film by using the proposed method. The energy depth of electrons trapped in the SiCN film is comparable with that in the silicon nitride and oxynitride films. It is suggested that the presence of such energetically deep trap centers in the SiCN films results in the long data

retention time in the SiCN-based memories. From the view point of the charge retention characteristics, the SiCN dielectric films can be employed as the charge trapping film of embedded NVMs. Hence, the SiCN dielectric film is a potential candidate which can replace silicon nitride film as the charge trapping film of embedded NVMs.

As described above, the dissertation proposes the constant-current carrier injection method and the analytical method for the charge retention characteristics in the charge trapping films. It was shown that the constant-current carrier injection method is useful for obtaining the accurate charge centroid of carriers trapped in the charge trapping films. The experimental results and discussion shown in this dissertation are important to get a better understanding of the hole trapping phenomena in the SiCN and silicon nitride charge trapping films. From the view point of the charge retention of NVMs, the proposed analytical method for the charge retention characteristics, which needs no adjustable and extra parameters, is very helpful for determining the energy distribution of carriers trapped in the SiCN or new dielectric films. The two methods proposed in the present study are considered to be advantageous to develop embedded NVMs employing the SiCN or new charge trapping films.

5.2 Future works

This dissertation revealed that the constant-current carrier injection method and the improved analytical method for charge retention characteristics are useful to have a better understanding of the charge trapping phenomena and the charge retention characteristics of NVMs.

In the present study, the SiCN and silicon nitride films of 31.6 and 30.4 nm in thickness were employed to obtain the clear hole trapping and the charge retention characteristics and to understand the movement of carriers in the charge trapping films. On the other hand, the thicknesses of charge trapping films ranging from 5 to 15 nm are used in the manufacturing industry of NVMs. Therefore, further study would be required to investigate the hole trapping and the charge retention characteristics in the charge trapping films with thicknesses ranging from 5 to 15 nm.

As was mentioned in section 1.2 in chapter 1, the SiCN-based charge trapping memory has higher programming and erasing speeds than the silicon nitride-based memory. However, in the present study, in chapter 2, almost the same $\Delta V_{fb,h}$-F_{inj} characteristics was obtained in both the SiCN and silicon nitride capacitors. The higher speed of hole injection in the SiCN capacitors compared to that in the silicon nitride capacitors might be a possible explanation for the high erasing speed in the SiCN capacitor. Further study on the carrier injection mechanism would be required to understand the programming and erasing operations in the SiCN-based memory.

In chapter 4, from the view point of the charge retention, it was suggested that the SiCN dielectric films can be employed for application in embedded NVMs. As was mentioned in chapter 1, the endurance is also an important feature of NVMs. Therefore, it will be essential to study the endurance characteristics of the SiCN-based NVMs.

Achievements

Achievements

A. Peer-reviewed Journal Papers

1. **Sheikh Rashel Al Ahmed**, Kaihei Kato, and Kiyoteru Kobayashi, "Hole trapping characteristics of silicon carbonitride (SiCN)-based charge trapping memories evaluated by the constant-current carrier injection method," Materials Science in Semiconductor Processing, 2017, *in press*.
    DOI: http://dx.doi.org/10.1016/j.mssp.2017.01.012

2. **Sheikh Rashel Al AHMED** and Kiyoteru KOBAYASHI, "Extraction of Energy Distribution of Electrons Trapped in Silicon Carbonitride (SiCN) Charge Trapping Films," IEICE TRANS. ELECTRON., 2017, Vol. E100-C, No. 7, pp. 662-668.
    DOI: http://doi.org/10.1587/transele.E100.C.662

B. Peer-reviewed Proceeding Papers

1. K. Kato, **S. R. A. Ahmed**, and K. Kobayashi, "Evaluation of Hole Trapping Characteristics in MONOS-Type Memories Using the Constant Current Carrier Injection Method," ECS Transactions, 2017, Vol. 75, No. 32, pp. 73-82.
   DOI: 10.1149/07532.0073ecst

2. **S. R. A. Ahmed**, K. Kato, and K. Kobayashi, "Experimental Extraction of the Charge Centroid in SiCN-Based Charge Trapping Memories Using the Constant-Current Carrier Injection Method," ECS Transactions, 2017, Vol. 75, No. 32, pp. 51-62.
   DOI: 10.1149/07532.0051ecst

3. **S. R. A. Ahmed**, S. Naito, and K. Kobayashi, "Characterization of Low-Dielectric Constant Silicon Carbonitride (SiCN) Dielectric Films for Charge Trapping Nonvolatile Memories," ECS Transactions, 2015, Vol. 69, No.3, pp. 99-109.
   DOI: 10.1149/06903.0099ecst

C. International Conference Presentations

1. **S. R. A. Ahmed**, K. Kato, and K. Kobayashi, "Experimental Extraction of the Charge Centroid in SiCN-Based Charge Trapping Memories Using the Constant-Current Carrier Injection Method," Ext. Abstr. MA2016-02(16): 1455, Pacific Rim Meeting on Electrochemical and Solid-State Science 2016 (The PRiME 2016 Meeting), October 2-7, 2016, Hawaii Convention Center and Hilton Hawaiian Village, Hawaii, USA.

2. K. Kato, **S. R. A. Ahmed**, and K. Kobayashi, "Evaluation of Hole Trapping Characteristics in MONOS-Type Memories Using the Constant Current Carrier Injection Method," Ext. Abstr. MA2016-02(16): 1464, Pacific Rim Meeting on Electrochemical and Solid-State Science 2016 (The PRiME 2016 Meeting), October 2-7, 2016, Hawaii Convention Center and Hilton Hawaiian Village, Hawaii, USA.

3. **S. R. A. Ahmed**, S. Tanaka, and K. Kobayashi, "Hole trapping characteristics of SiCN-based charge trapping memories using a constant-current carrier injection method," 7th International Symposium on Control of Semiconductor Interfaces (ISCSI-VII) International SiGe Technology and Device Meeting (ISTDM 2016)**,** FE-PB-10, June 7-11, 2016, Noyori Conference Hall, Nagoya University, Nagoya, Japan.

4. **S. R. A. Ahmed**, S. Tanaka, and K. Kobayashi, "Hole Trapping Characteristics of Nitride-Based Charge Trapping Memories Using the Constant-Current Carrier Injection Method," Ext. Abstr., pp. 27-28, International Workshop on Dielectric Thin Films for Future Electron Devices-Science and Technology-(2015 IWDTF), Session P Poster Session, P-8, November 2-4, 2015, Tokyo, Japan.

5. **S. R. A. Ahmed**, S. Naito, and K. Kobayashi, "Characterization of Low-Dielectric Constant Silicon Carbonitride (SiCN) Dielectric Films for Charge Trapping Nonvolatile Memories," Ext. Abstr. MA2015-02(16): 773, The 228th ECS Meeting, The Electrochemical Society, October 11-15, 2015, Phoenix Convention Center, Arizona, USA.